

(11) **EP 1 151 962 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:  
 07.11.2001 Bulletin 2001/45

(51) Int Cl.7: **B81C 3/00**, H01L 25/065,  
 H01L 23/48, G11B 19/20

(21) Application number: 00830314.1

(22) Date of filing: 28.04.2000

(84) Designated Contracting States:  
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU**  
**MC NL PT SE**  
 Designated Extension States:  
**AL LT LV MK RO SI**

- Ghironi, Fabrizio  
 20010 Bareggio (IT)
- Aina, Roberto  
 20010 Bareggio (IT)
- Bombonati, Mauro  
 20081 Abbiategrasso (IT)

(71) Applicant: STMicroelectronics S.r.l.  
 20041 Agrate Brianza (Milano) (IT)

(74) Representative: Cerbaro, Elena, Dr. et al  
**STUDIO TORTA S.r.l.**,  
 Via Viotti, 9  
 10121 Torino (IT)

(72) Inventors:  
 • Mastromatteo, Ubaldo  
 20010 Bareggio (IT)

(54) **Structure for electrically connecting a first body of semiconductor material overlaid by a second body of semiconductor material, composite structure using the electric connection structure, and manufacturing process thereof**

(57) The electric connection structure connects a first silicon body (10) to conductive regions (29, 30) provided on the surface of a second silicon body (1) arranged on the first body (10). The electric connection structure comprises at least one plug region (3) of silicon, which extends through the second body (1); at least one insulation region (2a, 8) laterally surrounding the plug region (3); and at least one conductive electromechanical connection region (23) arranged between the first body (10) and the second body (1), and in electrical

contact with the plug region (3) and with conductive regions (15-19; 40) of the first body (10). To form the plug region (3), trenches (2a) are dug in a first wafer (1) and are filled, at least partially, with insulating material (6). Next, the plug region (3) is fixed to a metal region (29) provided on a second wafer (10), by performing a low-temperature heat treatment which causes a chemical reaction between the metal and the silicon. Subsequently, the first wafer (1) is thinned until the trenches (2a) and electrical connections (29, 30) are formed on the free face of the first wafer.

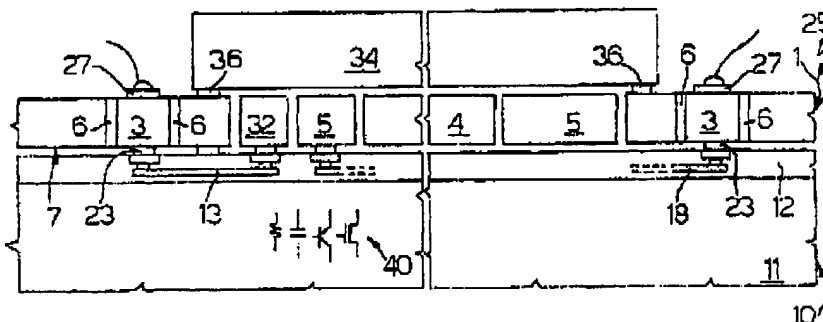


Fig.8

EP 1 151 962 A1

Printed by Jouve, 75001 PARIS (FR)

**BEST AVAILABLE COPY**

1

EP 1 151 962 A1

2

**Description**

[0001] The present invention regards a structure for electrically connecting a first body of semiconductor material overlaid by a second body of semiconductor material, a composite structure using the electric connection structure and a manufacturing process.

[0002] In particular, the invention can be used for electrically connecting a first silicon wafer incorporating electronic components to a second silicon wafer incorporating a micromechanical structure and/or to the outside. The invention can likewise be used for electrically connecting the first wafer to a third body carried by the second wafer, as well as for connecting the first wafer to the outside when the first wafer is covered by a protection structure, and thus is not directly accessible. An example of a particular application is represented by a micro-electromechanical system including a first wafer incorporating a circuit for controlling the parameters defining the state of a micro-electromechanical structure (for example, the position of a microactuator); a second wafer incorporating the micro-electromechanical structure; and a third wafer forming a cap for protecting the micro-electromechanical structure.

[0003] Various techniques are known for mechanically connecting two semiconductor material bodies (see, for example, Martin A. Schmidt, "Wafer-to-Wafer Bonding for Microstructure Formation", Proceedings of the IEEE, Vol. 85, No. 8, August 1998). However, such techniques do not enable two or three wafers to be electrically connected, in addition to be mechanically connected, or covered components of one of the wafers to be electrically accessed.

[0004] The aim of the present invention is to provide a connection structure that enables semiconductor material bodies made on different substrates to be overlaid and to be connected mechanically and electrically together and to the outside.

[0005] According to the present invention an electric connection structure, a composite structure, and a process for manufacturing a composite structure are provided, as defined in Claims 1, 12, and 22, respectively.

[0006] For a better understanding of the present invention, preferred embodiments thereof are now described, merely to provide non-limiting examples, with reference to the attached drawings, wherein:

- Figures 1 and 2 are cross-sections through a semiconductor material wafer, in two successive manufacture steps, according to a first embodiment of the invention;
- Figure 3 shows a cross-section through the wafer of Figure 2, after bonding to a second semiconductor material wafer;
- Figures 4-6 show a cross-section of the multiwafer structure of Figure 3, in successive manufacture steps;
- Figure 7 is a perspective view of the left-hand half

of the multiwafer structure of Figure 8;

- Figure 8 shows a cross-section of the multiwafer structure of Figure 6, in a final manufacture step;
- Figures 9-11 show a cross-section of a micro-electromechanical system according to a second embodiment of the invention;
- Figure 12 shows a cross-section of a composite structure formed starting from three semiconductor material substrates, according to a third embodiment of the invention;
- Figures 13 and 14 show cross-sections of a semiconductor material wafer, in two successive manufacture steps according to a fourth embodiment of the invention;
- Figure 15 shows a cross-section of the wafer of Figure 14 after bonding to a second semiconductor material wafer;
- Figure 16 shows a cross-section of a composite structure obtained from the double wafer of Figure 15, in a subsequent manufacture step;
- Figure 17 shows a cross-section of a composite wafer, according to a fifth embodiment of the invention; and
- Figures 18 and 19 show cross-sections of a composite wafer, according to a sixth embodiment of the invention, in two successive manufacture steps.

[0007] Figures 1-8 show a first embodiment of a process for manufacturing a micro-electromechanical system including a control and sensing circuitry and a micro-electromechanical sensor, for example an accelerometric sensor.

[0008] Initially, Figure 1, a first wafer 1 of semiconductor material, typically P<sup>++</sup> or N<sup>++</sup> doped monocrystalline silicon, sectioned along two parallel half-planes, so as to show different areas in the left-hand half and in the right-hand half, is masked and etched to form first deep trenches 2a. For example, the first wafer 1 may have a conductivity of between 5 and 15 mΩ/cm, preferably 10 mΩ/cm. As shown in Figure 2, the first trenches 2a have a closed shape and enclose monocrystalline silicon plug regions 3 intended to form through connections, as explained more clearly hereinafter.

[0009] Subsequently, the first trenches 2a are filled, either completely or partially, with insulating material 6, for example silicon dioxide. To this end, a silicon dioxide layer is deposited or grown, and is subsequently removed from a first surface 7 of the first wafer 1, to obtain the structure shown in Figure 2.

[0010] Next, Figure 3, the first wafer 1 is bonded to a second wafer 10 comprising a monocrystalline silicon substrate 11 and an insulation and/or passivation layer 12. In particular, the substrate 11 houses conductive and/or insulating regions forming electronic components for biasing the accelerometric sensor 8 and for detecting and processing electrical signals generated by the accelerometric sensor 8. As an example, Figure 3 shows conductive regions 15-16 of the N/P-type be-

3

EP 1 151 962 A1

4

longing to an electronic circuit 40, which is shown only schematically. In addition, the insulation and/or passivation layer 12 houses metal regions 13, 18, which terminate, at one or both of their ends, with pad regions 19 facing the surface 22 of the second wafer 10.

[0011] Connection regions 23 are provided on the surface 22 of the second wafer 10, on top of the pad regions 19, and are of a metal that is able to react at a low temperature with the silicon of the first wafer 1 to form a gold/silicon eutectic or a metallic silicide. Typically, the connection regions 23 are made of gold, in the case where the aim is to obtain a eutectic, or of a metal chosen from among the group comprising palladium, titanium, and nickel, in the case where the aim is to obtain a silicide. Bonding regions 24 are also provided on the surface 22 and are preferably formed at the same time as the connection regions 23.

[0012] For bonding the first wafer 1 to the second wafer 10, the first wafer 1 is turned upside down so that the first surface 7 of the first wafer 1 faces the second wafer 10. The plug regions 3 of the first wafer 1 are brought into contact with the connection regions 23 of the second wafer 10, and subsequently a heat treatment at low temperature, for example 350-450°C, is carried out for a period of 30-45 min., so that the metal of the connection regions 23 of the second wafer 10 react with the silicon of the plug regions 3 and form a metallic silicide which bonds the first and the second wafers 1, 10. Thereby, a double wafer 25 is obtained, as shown in Figure 3.

[0013] Subsequently, Figure 4, the first wafer 1 is thinned from the back mechanically, for example by grinding, preferably so as to obtain a thickness of 30-40 µm. The first wafer 1 then has a second surface 26 opposite to the first surface.

[0014] Next, Figure 5, a metal layer (for example, an aluminum layer) is deposited and defined, so as to form metal regions 27 extending above the plug regions 3 and in direct electrical contact with the latter.

[0015] Subsequently, the first wafer 1 is masked and etched so as to form second trenches 2b defining an accelerometric sensor 8. In particular, as may be seen in Figures 6 and 7, the second trenches 2b separate a mobile region (forming a rotor 4) and a fixed region (forming a stator 5) from the rest of the wafer 1 and from one another. The rotor 4 is connected, through elastic-connection regions (also referred to as springs 31) to fixed biasing regions 32, which are set in areas corresponding to respective connection regions 23, connected, through the metallic regions 13, to the plug regions 3.

[0016] Next, Figure 8, a cap element 34 is fixed to the wafer 1 through adhesive regions 36, in a per se known manner, and then the double wafer 25 is cut into individual dice. Finally, the metal region 27 is contacted applying the usual wire-bonding technique.

[0017] Thereby, the connection regions 23 ensures mechanical connection between the monocrystalline silicon wafers 1 and 10 and electrical connection between

the surface 22 of the second wafer 10 and the plug regions 3. In turn, the plug regions 3 allow the second wafer 10 to be contacted from above. In particular, some plug regions 3 enable the second wafer 10, not directly accessible from the front, to be connected to the outside, without requiring costly processes to be carried out from the back. In addition, as is shown in the left-hand half of Figure 8, this solution also enables connection of regions formed in the first wafer 1 to the outside. Here the rotor 4 is connected to the outside through a first connection region 23 (beneath the biasing region 32), a metal region 13, a second connection region 23 (beneath the plug region 3), and the plug region 3. The plug regions 3 are insulated by insulation regions formed by the insulating material 6 and possibly by the air present in the first deep trenches 2a, and are thus electrically insulated from the rest of the first wafer 1, except, obviously, for the regions connected to them via electric connection lines 30.

[0018] With the solution of Figures 1-8 a pressure sensor, instead of an accelerometric sensor, may be formed.

[0019] Figures 9-11 show a second embodiment of the invention regarding a unit for micrometric regulation of the read/write head of a hard-disk driver. In detail, initially the same steps are carried out as described previously with reference to Figures 1-4. After thinning the first wafer 1, an oxide layer 35 is deposited and removed selectively at the plug regions 3 to form openings 28. The second trenches 2b are then formed through the oxide layer 35 and through the wafer 1.

[0020] Subsequently, an insulating layer 38 is deposited, for example a stick foil which does not enter the second trenches 2b. The insulating layer is removed from above the openings 28, and metal connection regions are formed by depositing and defining a metal layer. In particular, in the illustrated example the metal layer fills the openings 28, where it forms contacts 29. In addition, an electric connection line 30 is formed and extends from the contact 29 arranged above the plug region 3 furthest to the right, up to above the rotor 4.

[0021] Subsequently, the composite wafer 25 is cut into dice, the insulating layer 38 is removed in oxygen plasma, and a ceramic body, referred to as slider 41, is bonded to the rotor 4 in a per se known manner (Figure 11). The slider 41 carries a transducer 42 for data reading/writing on a hard disk (not shown). The transducer 42 is electrically contacted through connection regions 43, one of which may be seen in Figure 11, which are formed directly on one side of the slider 41. Each connection region 43 extends from the transducer 42 as far as a pad 44 in electrical contact with an electric connection line 30.

[0022] Thereby, the plug region 3 furthest to the right enables electrical connection between the transducer 42 on the slider 41 and the electrical circuit 40, which can thus transmit to the transducer 42 the data to be written, or process the signal picked up by the transducer.

3

5

EP 1 151 962 A1

6

er 42. In addition, in a known manner, the electrical circuit 40 controls movement of the rotor 4, and consequently of the slider 41. Finally, a connection via an intermediate plug region (not shown) enables connection of the electrical circuit 40 to the outside, in a way similar to that illustrated in the right-hand part of Figure 8.

[0023] Consequently, also in this case the plug regions 3 enable connection of non-accessible regions of the second wafer 10 to elements arranged above them (here, the transducer 42), as well as to the outside.

[0024] Figure 12 shows a third embodiment regarding the manufacture of circuits or structures to be kept in vacuum conditions. In the illustrated example, the wafer 1, after forming the plug regions 3 by digging the first trenches 2a and filling them with insulating material 8, has been bonded to a second wafer 10, wherein a filter 48 has been previously made, for example of the band-pass type for high frequencies. The first wafer 1 is bonded to the second wafer 10, not only through the connection regions 23, but also through a sealing region 49 which extends between the first wafer 1 and the second wafer 10, and completely surrounds the area in which the filter 48 is formed, as well as the plug regions 3. The sealing region 49 is, for example, made using a low-melting glass and has a closed shape. If bonding of the first wafer 1 and second wafer 10 is carried out in a low-pressure environment, the filter 48 remains vacuum encapsulated.

[0025] Next, the first wafer 1 is thinned as described above, and the double wafer 1, 10 is cut into dice 50. The dice 50 are then bonded to a third wafer 51 which houses a circuit 52 and which has previously been provided with connection regions 23a similar to the connection regions 23. The thinned side of the first wafer 1 faces the third wafer 51, and the plug regions 3 must be aligned to the connection regions 23a.

[0026] In this case, the first wafer 1, in addition to protecting and isolating the filter 48 from the outside environment and maintaining it in vacuum conditions, enables its electrical connection with the circuit 52 incorporated in the third wafer 51. In addition, it is possible to carry out electrical testing of the circuit 52 connected to the filter 48 at the wafer level (EWS-Electric Wafer Sort test).

[0027] Figures 13-16 show a fourth embodiment of the invention. According to Figure 13, initially the first wafer 1 comprises a substrate 53 accommodating first trenches 72a, and the first trenches 72a are filled with insulating material 78 to insulate first plug portions 73. In a way similar to that described with reference to Figure 1 for the plug regions 3. Then a sacrificial layer 54, for example of silicon dioxide, is deposited or grown, then is masked and etched so as to form openings 55 on top of the first plug portions 73 and in areas where anchorages with the structure on top are to be made, as described hereinafter.

[0028] Subsequently (Figure 14), a polycrystalline silicon seed layer is deposited on top of the sacrificial layer

54 and in the openings 55, and then a polycrystalline silicon epitaxial layer 58 is grown. In this way, the epitaxial layer 58 is in direct contact with the substrate 53 at the openings 55. Next, inside the epitaxial layer 58 third and fourth trenches 60a, 60b are dug, which reach as far as the sacrificial layer 54.

[0029] In particular, the third trenches 60a delimit second plug portions 62 aligned vertically with the first plug portions 73 in the substrate 53, and the third trenches 60a define a desired micromechanical structure (in the example illustrated, a microactuator 57 of the rotating type, comprising a rotor 58 and a stator 59, with the rotor 58 supported by springs, which are not illustrated).

[0030] Subsequently, in a known way, a part of the sacrificial layer 54 is removed through the fourth trenches 60b. In particular, the sacrificial layer 54 is removed beneath the rotor 58 to form an air gap 63, and it substantially remains underneath the stator 59. The sacrificial layer 54 is removed only to a very small extent through the third trenches 60a, given the different geometry (the micromechanical structure is formed by thin regions and/or perforated regions, allowing the sacrificial layer 54 to be substantially removed; this, instead, is not done through the third trenches 60a).

[0031] In a way not shown, it is then possible to fill the third trenches, at least partially, with insulating material, in a way similar to that described for the first trenches 2a of Figure 1.

[0032] Subsequently (Figure 15), the first wafer 1 is turned upside down and bonded to the second wafer 10, inside which components of the circuit 40 have already been formed, and on top of which the connection regions 23 have already been made. Also in this case, a low-temperature heat treatment is carried out to enable a chemical reaction between the silicon of the epitaxial layer 56, at the second plug portions 62, and the metal of the connection regions 23. Next, the substrate 53 of the first wafer 1 is thinned until the insulating material 76 (or at least the bottom of the first trenches 72a) is reached, an oxide layer 35 is deposited, the openings 28 are formed in the oxide layer 35, and then second trenches 72b are made which separate fixed parts from mobile parts in the substrate 53.

[0033] Next, as has been described with reference to Figure 10, an insulating layer (stick foil) is deposited and selectively removed, and the electrical contacts 29 and electric connection lines 30 are formed. In Figure 16, an electric connection line 30 connects the portion of the substrate 53 to which the rotor 58 is anchored (cap region 67) to the first plug region 73 that is furthest to the left, thus enabling electrical connection of the rotor 58 to the circuit 40 through the cap region 67, the first plug portion 73 on the left, and the second plug portion 62 on the left. Shown in the right-hand half of Figure 16 is instead the electrical connection between the circuit 40 and the outside, through the second plug portion 62, the first plug region 73, and the connection region 23 on the right.

7

EP 1 151 982 A1

8

[0034] Subsequently, the insulating layer is removed, and a body to be moved, for example a slider similar to the slider 41 of Figure 11, can be fixed to the cap region 87.

[0035] The solution shown in Figures 13-16 thus provides a micromechanical structure 57 protected by a cap (cap region 87) and easily connects the circuit 40 both to the micromechanical structure 57 and to the outside.

[0036] Figure 17 shows a variation of the structure of Figure 16, in which the rotor 58 is not anchored to the substrate 53, but is supported by springs (not shown) and biasing regions 60, similar to the biasing regions 31, 32 of Figure 7. In addition, the cap region 87 is fixed and does not have the second trenches 72b. The rotor 58 and stator 59 are connected via connection regions 23 and pad regions 19 to metallic regions 13, 18 formed in the second wafer 10. The metallic regions 13 are connected to the outside (as shown in the left-hand half of Figure 17) via further connection regions 23 aligned with plug regions 62, 73 formed in the first wafer 1, in a way similar to that described with reference to Figures 13-16, and via contacts 29. In addition, the metallic regions 18 enable connection of the circuit 40 to the stator 59 and, via plug regions 62, 73 and contacts 29, to the outside, as shown in the right-hand half of Figure 17. An insulating layer 80 covers the surface 26 of the first wafer 1.

[0037] Figures 18 and 19 show a sixth embodiment, in which a micromechanical structure, for example an accelerometric sensor 8, is protected by a cap and electrically connected to the biasing and sensing circuit via plug regions.

[0038] Initially (Figure 18), the first wafer comprises a substrate 53, which, in contrast to the previous embodiments, is not etched to form trenches. On the substrate 53, a sacrificial layer 54 is deposited and defined, and is removed only at openings 55. Next, a polycrystalline silicon seed layer is deposited, and the epitaxial layer 56 is grown, as described with reference to Figure 14.

[0039] The epitaxial layer 56 is etched to form fifth trenches 65a for delimiting second plug portions 64. Here, the fifth trenches 65a are filled, either partially or completely, with insulating material 66, sixth trenches 65b are formed for defining the accelerometric sensor 8, and the sacrificial layer 54 is partially removed through the sixth trenches 65b, so as to free the rotor 58 of the accelerometric sensor 8. As for the embodiment shown in Figures 1-8, the rotor 58 is carried by the fixed part via springs (not illustrated).

[0040] Subsequently, the first wafer 1 is bonded to the second wafer 10 using the connection regions 23 already formed on the surface 22 of the second wafer 10. Then the first wafer 1 is thinned by grinding until the desired thickness for the substrate 53. Next, the substrate 53 is selectively removed so as to form a cap region 87 of larger dimensions than the rotor 58, but of smaller dimensions than the chip housing the circuit 40, obtained after cutting the wafers 1, 10. In this way, the cap region 87 covers the rotor 58 from the back (protecting

it mechanically), but leaves the plug regions 64 free.

[0041] Finally, the contacts 29 and the electric connection lines 30 are formed, which, in this embodiment, contact directly the silicon of the epitaxial layer 54. In particular, in the example illustrated in Figure 19, an electric connection line 30 connects a region (not shown), arranged inside the fixed part and is electrically connected to the rotor 58, to the plug region 64 on the left, and thus to the circuit 40. A ball-and-wire connection on the right instead enables connection of the circuit 40 to the outside.

[0042] When the accelerometric sensor 8 is to be kept at low pressure, for example to reduce friction with air during movement, a sealing region 49 may be provided which surrounds the area of the accelerometric sensor 8, then the first wafer 1 may be bonded to the second wafer 10 in vacuum conditions, as already described with reference to Figure 12.

[0043] The advantages of the process and structures described are evident from the above. In particular, it is emphasized that they enable mechanical connection of two bodies of semiconductor material, in particular of monocrystalline silicon, arranged on one another, and at the same time the electrical connection of a structure or circuit formed in the underlying body (covered by the overlying body) to the outside or to a structure made in the overlying body; or else, they enable electrical connection of the underlying body to regions arranged above the overlying body, without requiring complicated and costly processes to be carried out from the back, without damaging the structures and circuits already made, and applying single manufacture steps that are commonly used in the manufacture of wafers of semiconductor material for forming micro-electromechanical structures.

[0044] The described solutions moreover make it possible, when necessary, to isolate preset areas of the underlying body and/or of the overlying body from the outside environment, for example to enclose delicate elements in a low-pressure environment, and/or to isolate and prevent contamination of these elements during manufacture (for example, cutting semiconductor material wafers), during subsequent manipulation steps, and during use.

[0045] Finally, it is clear that numerous modifications and variations may be made to the connection structure, the composite structure, and to the manufacture process described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. In particular, it is emphasized that the present connection structure may be used for a wide range of applications, both for the connection of electronic circuits integrated in two or more different substrates, and for the connection of micro-electromechanical structures of various kinds to biasing/control/sensing circuits associated to the micro-electromechanical structures. The present connection structure may be used for connecting a high number of substrates, according to the re-

9

EP 1 151 962 A1

10

quirements and to general considerations of a mechanical/electrical nature.

#### Claims

1. An electric connecting structure for connecting a first body (10) of semiconductor material overlaid by second body (1) of semiconductor material, characterized by:

at least one plug region (3; 73, 62; 64) extending through a portion of said second body (1) and made of semiconductor material;  
at least one insulation region (2a, 6; 60a, 72a, 76; 65a, 66) surrounding laterally said plug region (3; 73, 62; 64); and  
at least one first electromechanical connection region (23) of electrically conductive material arranged between said first body (10) and said second body (1) and in electrical contact with said plug region (3; 73, 62; 64) and with conductive regions (15-19; 40) of said first body (10).

2. The electric connection structure of Claim 1, characterized in that said plug region (3; 62, 73) extends throughout the thickness of said second body (1) and has a first face and a second face, said first face being in contact with said first electromechanical connection region (23); and comprising at least one contact region (27; 29; 23a) of electrically conducting material, in contact with said second face of said plug region.

3. The electric connection structure of Claim 2, characterized by an electric connection line (30) extending above said second body (1) and having a first end forming said contact region (29).

4. The electric connection structure of Claim 3, characterized in that said electric connection line (30) has a second end in electrical contact with a conductive region of said second body (1).

5. The electric connection structure of Claim 3, characterized in that said electric connection line (30) has a second end in electrical contact with a contact region (44) formed on a third body (41) fixed to said second body (1).

6. The electric connection structure of Claim 2, for electrically connecting said second body (1) to a third body (51) of semiconductor material arranged on said second body (1), characterized in that said contact region comprises at least one second electromechanical connection region (23a) made of a material resulting from the chemical reaction of said

semiconductor material with a metal, said second electromechanical connection regions (23a) being arranged between said second body (1) and said third body (51).

7. The electric connection structure of Claim 1, for a second body (1) comprising a substrate region (53) and an epitaxial region (56) arranged on each other and partially insulated from one another by insulating regions (54, 63), characterized in that said plug region (62, 73) comprises a first plug portion (73) extending throughout the thickness of said substrate region (53), and at least one second plug portion (62) formed inside said epitaxial region (56), said second plug portion (62) being aligned and in direct electrical contact with said first plug portion (73);

said insulation region (60a, 72a, 76) comprises a first insulation portion (72a, 76) laterally surrounding said first plug portion (73), and a second insulation portion (60a) laterally surrounding said second plug portion (62);  
at least one contact region (29) of electrically conducting material extends on a free face (28) of said substrate region (53) in electrical contact with said first plug portion (73);  
and said second plug portion (62) faces and is in direct electrical contact with said first electromechanical connection region (23).

8. The electric connection structure of Claim 1, for a second body (1) comprising a substrate region (67) and an epitaxial region (56) arranged on one another and reciprocally insulated by insulating regions (54, 63), characterized in that said substrate region (67) has a smaller area than said epitaxial region (56), said plug region (64) extends throughout the thickness of said epitaxial region (56), is not aligned with respect to said substrate region (67), and has a first face and a second face, said first face being in contact with said first electromechanical connection region (23), and said second face being in direct contact with at least one electric connection region (30) of electrically conducting material.

9. The electric connection structure according to any of the foregoing claims, characterized in that said insulation region (2a, 6; 60a, 72a, 76; 65a, 66) comprises a trench having a closed shape filled at least partially with insulating material (6; 66; 76).

10. The electric connection structure according to any of the foregoing claims, characterized in that said first electromechanical connection region (23) is made of a material resulting from the chemical reaction of said semiconductor material with a metal.

11

EP 1 151 962 A1

12

11. The electric connection structure according to any of the foregoing claims, characterized in that said first electromechanical connection region (23) is made of a metal resulting from the chemical reaction of silicon with a metal chosen from among a group comprising gold, palladium, titanium, and nickel.

12. A composite structure comprising a first body (1) of semiconductor material, a second body (10) of semiconductor material arranged on said first body (1), and an electric connection structure, characterized in that said electric connection structure is formed according to any of Claims 1-11.

13. A composite structure comprising a first body (10) of semiconductor material, a second body (1) of semiconductor material arranged on said first body (10), and an electric connection structure according to Claim 2, characterized in that said first body (10) houses an electronic circuit (15-19; 40), and said second body (1) houses a micro-electromechanical device (8; 57) comprising a fixed part (1, 5, 32; 58, 59, 68) and a mobile part (4; 58) separated from each other by at least one delimitation trench (2b) extending through said second body (1).

14. The composite structure of Claim 13, characterized in that an external electric connection wire is bonded to said contact region (29).

15. The composite structure of Claim 13, characterized in that said electric connection structure comprises an electric connection line (30) extending above said second body (1) and having a first end forming said contact region (29), and a second end in electrical contact with said micro-electromechanical device (8; 57).

16. The composite structure of Claim 13, characterized by a third body (41) fixed to said second body (1), said electric connection structure comprising an electric connection line (30) having a first end forming said contact region (29) and a second end in electrical contact with a contact region (44) formed on said third body (41).

17. The composite structure of Claim 16, characterized in that said third body (41) is a slider, and in that said composite structure forms an actuator unit for micrometric position regulation of a hard-disk driver.

18. A composite structure comprising a first body (10) of semiconductor material, a second body (1) of semiconductor material arranged on said first body, a third body (51) of semiconductor material fixed to said second body, and an electric connection struc-

ture according to Claim 6, characterized in that said first body (10) and said third body (51) house a respective electronic circuit (48, 52), said electronic circuits being connected together through said plug region (3).

19. The composite structure of Claim 18, characterized by a sealing region (49) having a closed shape and arranged between said first and said second bodies (10, 1), outside said electronic circuit (48).

20. A composite structure comprising:

a first body (10) of semiconductor material;  
a second body (1) of semiconductor material arranged on said first body and comprising a substrate region (53) and an epitaxial region (56), overlaid to each other and partially insulated from one another by insulating regions (54, 63); and  
an electric connection structure according to Claim 7,

characterized in that said epitaxial region (56) houses a micro-electromechanical device (57) comprising a fixed part (59, 68) and a mobile part (58) separated from one another by at least one delimitation trench (80b) extending through said epitaxial region (56), and in that said substrate region (53) forms a cap region (67).

21. A composite structure comprising:

a first body (10) of semiconductor material;  
a second body (1) of semiconductor material arranged on said first body and comprising a substrate region (67) and an epitaxial region (58), overlaid to each other and insulated from one another by insulating regions (54, 83), said substrate region (67) having a smaller area than said epitaxial region (58); and  
an electric connection structure according to Claim 8,

characterized in that said epitaxial region (56) houses a micro-electromechanical device (8) comprising a fixed part (59) and a mobile part (58) separated from one another by at least one delimitation trench (65b) extending through said epitaxial region (56), and in that said substrate region forms a cap region (67) which has larger dimensions than said mobile part (58) and is fixed to said fixed part (59).

22. A process for manufacturing a composite structure, characterized by the steps of:

forming at least one plug region (3; 73, 82; 84)

13

EP 1 151 962 A1

14

surrounded by an insulation region (2a, 6; 60a, 72a, 76; 85a, 86) extending through a first wafer (1) of semiconductor material;  
forming at least one electromechanical-connection region (23) of conductive material on a second wafer (10) of semiconductor material, and aligned with said plug region;  
bringing said first wafer (1) and said second wafer (10) close together, bringing said plug region (3; 73, 82; 84) into contact with said electromechanical-connection (23); and  
fixing said first wafer and said second wafer through said electromechanical connection region.

23. The process of Claim 22, characterized by the steps of:

Initially forming said insulation region (2a, 6) in said first wafer (1), said insulation region partially extending inside said first wafer from a surface (7) of said first wafer and laterally delimiting said one plug region (3);  
turning said first wafer (1) upside down to bring said surface (7) of said first wafer in a facing position with said second wafer (10); and  
thinning said first wafer (1) until said insulation region (2a, 6).

24. The process of Claim 23, characterized in that said step of forming said insulation region (2a, 8) comprises the steps of:

forming isolation trenches (2a) in said first wafer (1); and  
at least partially filling said isolation trenches with insulating material (8).

25. The process of Claim 24, characterized by the step of forming trenches (2b) delimiting a micro-electromechanical structure (8) in said first wafer (1), and forming an electronic circuit (13-19) in said second wafer (10) before forming said electromechanical-connection region.

26. The process of Claim 22, characterized by the steps of:

forming a first insulation portion (72a, 76) of said insulation region in a substrate (53) of semiconductor material, said first insulation portion (72a, 76) partially extending inside said substrate from a surface of said substrate, and laterally delimiting a first plug portion (73) of said plug region;  
growing an epitaxial layer (56) from said surface of said substrate (53);  
forming at least one second insulation portion

(60b) of said insulation region in said epitaxial layer (56), said second insulation portion (60b) extending throughout the thickness of said epitaxial layer and  
delimiting a second plug portion (82) of said plug region which is substantially aligned and in electrical contact with said first plug portion (73);  
fixing said second plug portion (82) to said second wafer (10);  
thinning said substrate (53) until said first insulation portion (72a, 76); and  
forming contact regions (29, 30) on a free face of said substrate (53).

27. The process of Claim 22, characterized by the steps of:

on a substrate (53), growing an epitaxial layer (56);  
forming said insulation region (85a, 86) in said epitaxial layer (56), said insulation region (85a, 86) extending throughout the thickness of said epitaxial layer and delimiting said plug region (84);  
forming a device (57) to be protected in said epitaxial layer (56);  
fixing said epitaxial layer (56) of said first wafer (1) to said second wafer (10) through said plug region (84); selectively removing said substrate (53) to form a cap region (67) covering said device (57) to be protected, and freeing said plug region (84); and  
forming contact regions (29, 30) above said plug region (84).

28. The process according to any of Claims 22-27, characterized in that said step of fixing said first wafer (1) to said second wafer (10) is carried out in vacuum conditions and further comprises the step of forming a sealing region (49) between said first wafer (1) and said second wafer (10).

29. The process according to any of Claims 22-28, characterized in that said conductive material of said electromechanical connection region (23) is a metal, and in that said fixing step comprises the step of causing said metal of said electromechanical-connection structure (23) to react with said semiconductor material of said plug region (3; 82; 84).



EP 1 151 962 A1

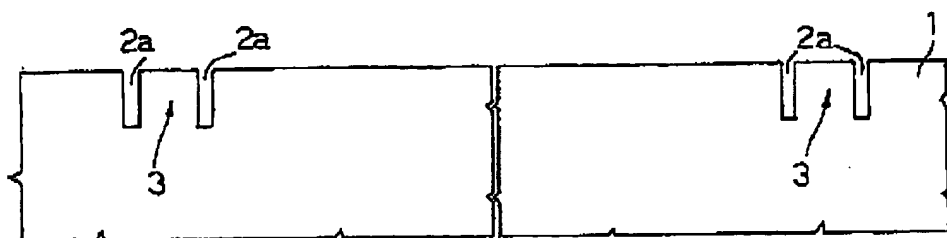


Fig. 1

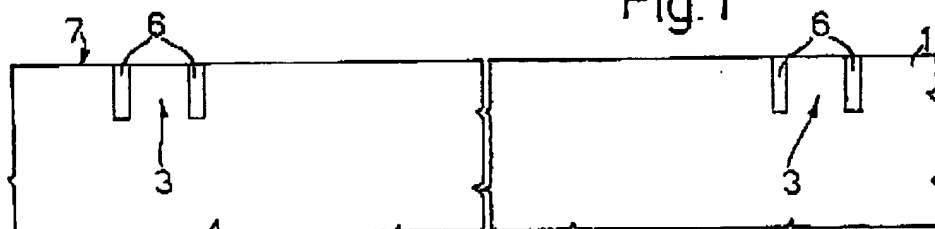


Fig. 2

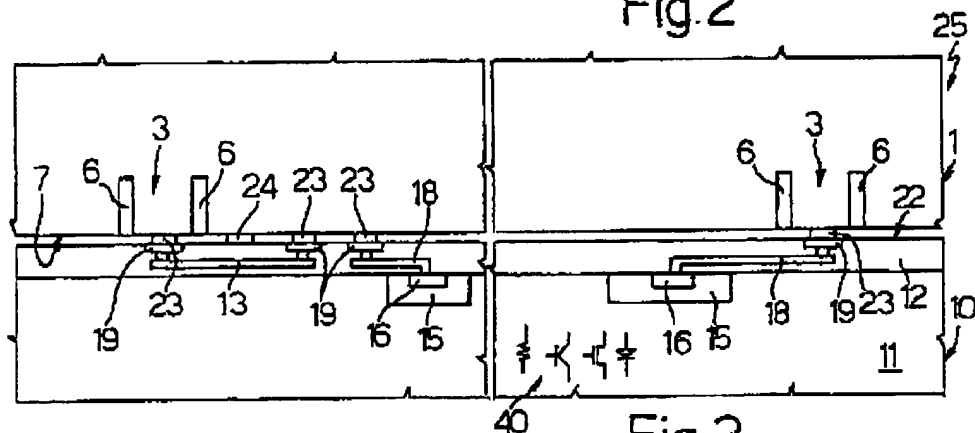


Fig. 3

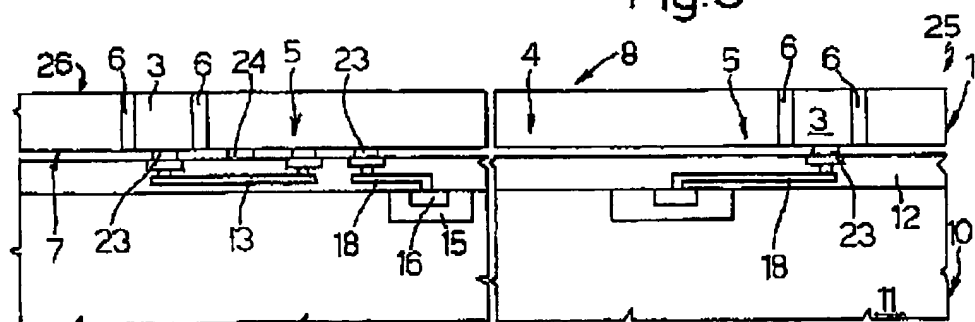


Fig. 4

EP 1 151 962 A1

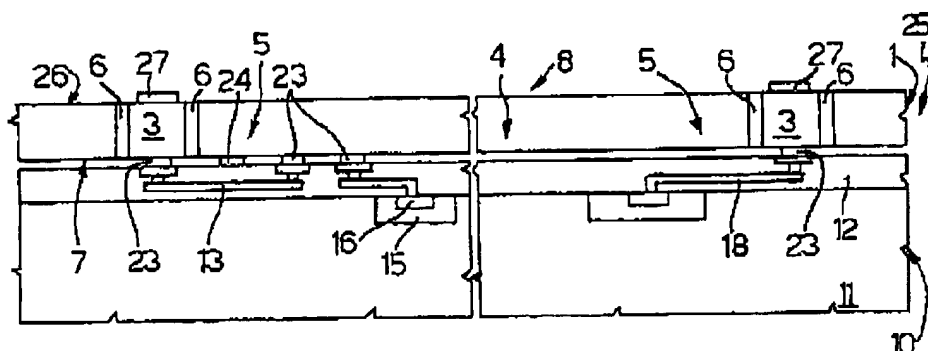


Fig.5

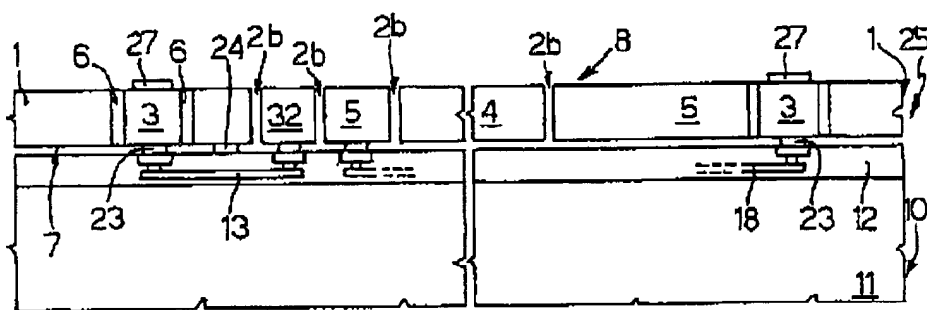


Fig.6

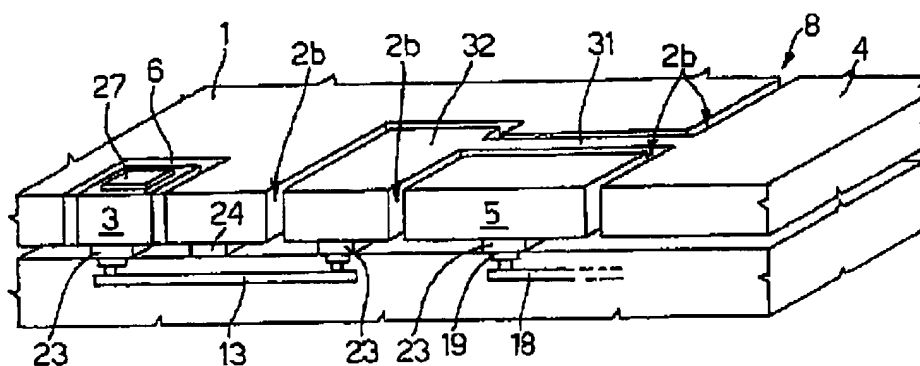


Fig.7

**EP 1 151 962 A1**

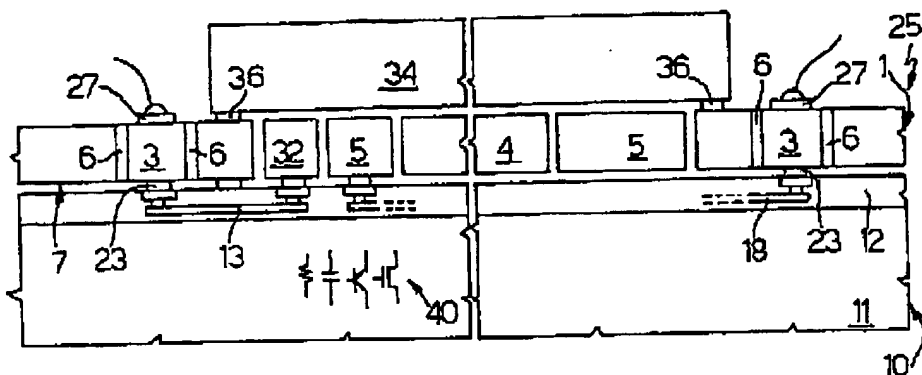


Fig.8

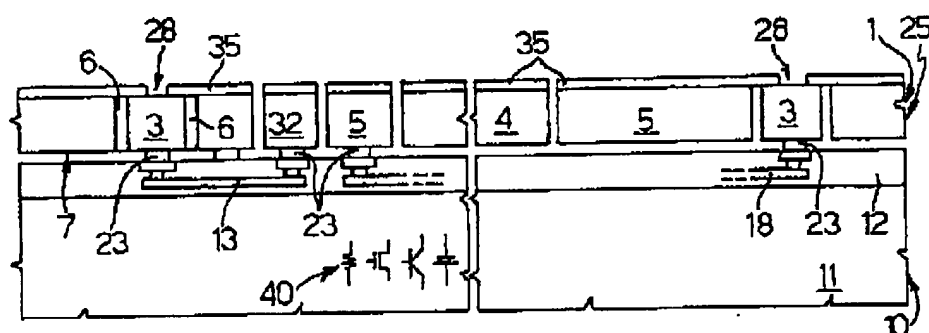


Fig.9

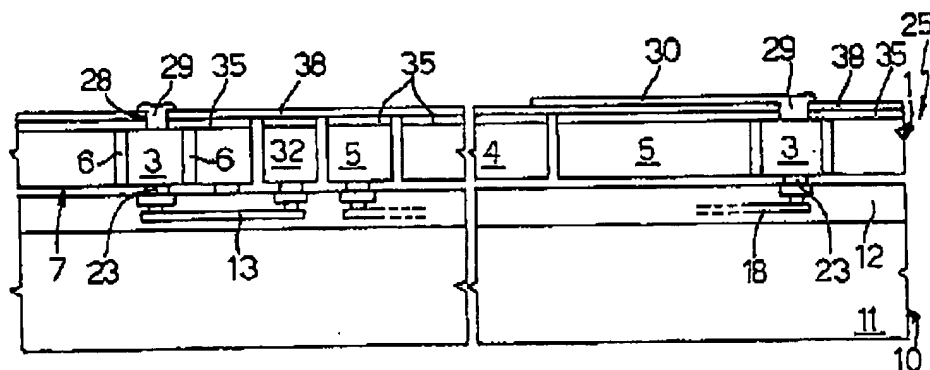


Fig.10

**EP 1 151 962 A1**

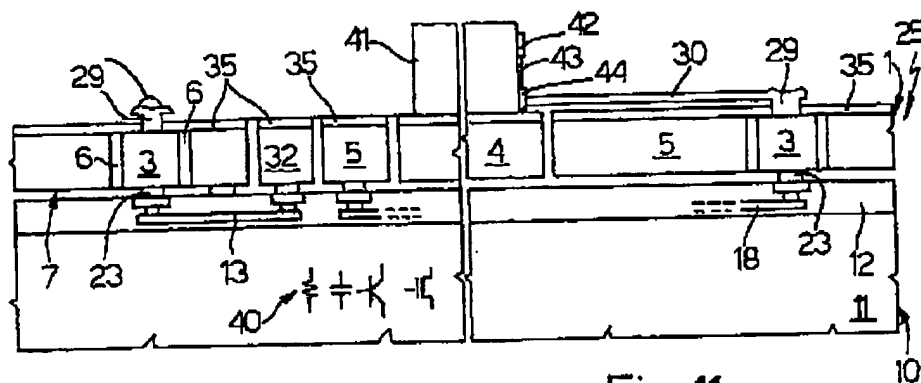


Fig. 11

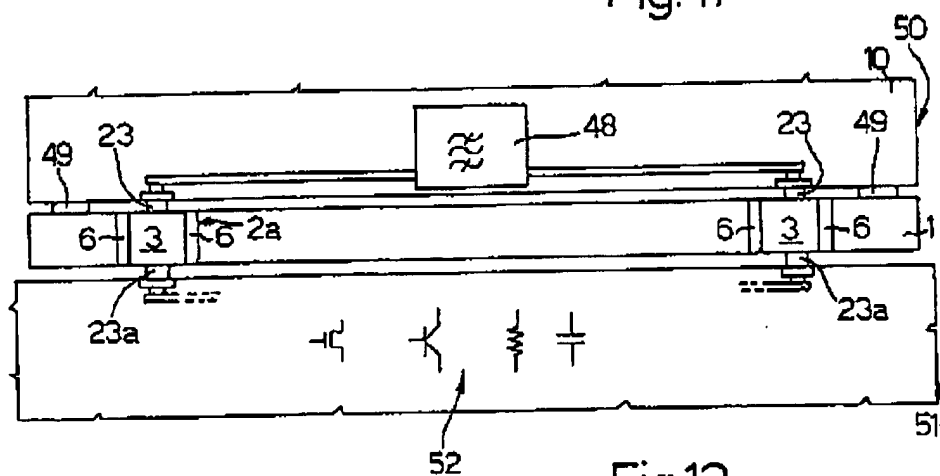


Fig.12

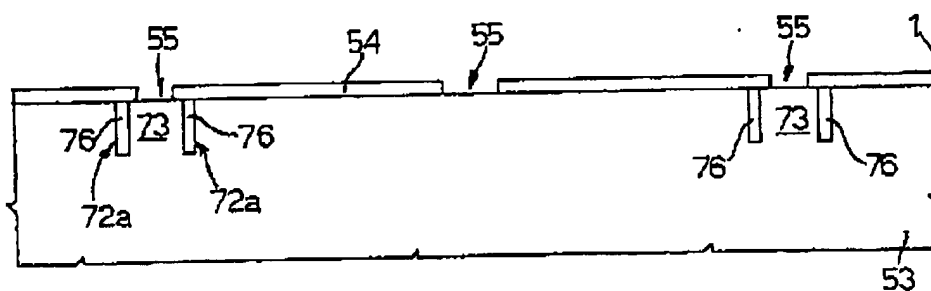


Fig.13

**EP 1 151 962 A1**

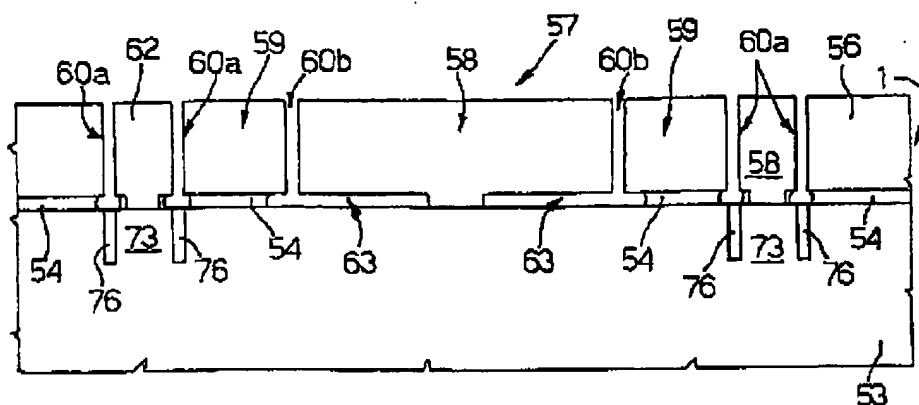


Fig.14

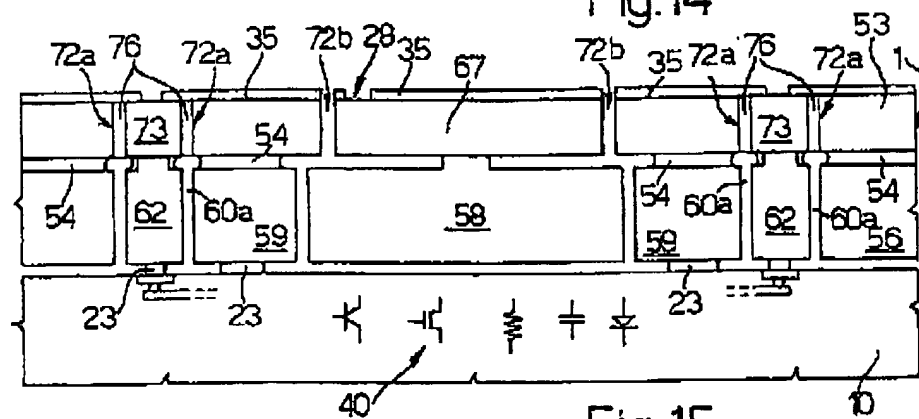


Fig. 15

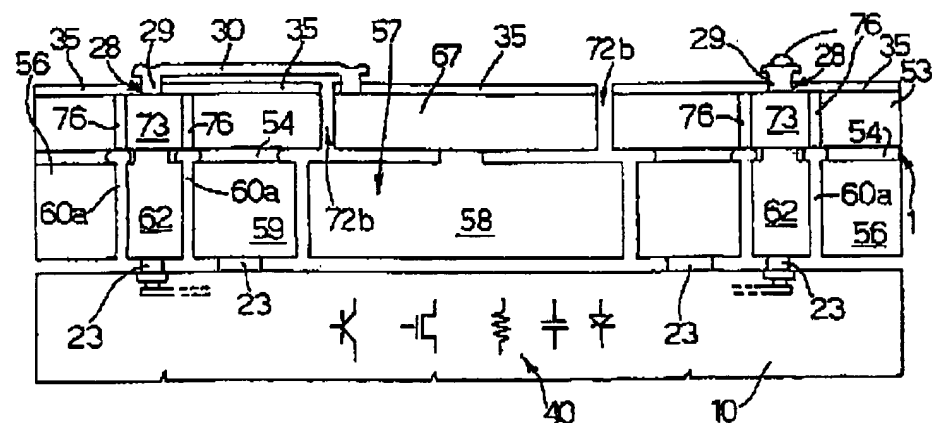


Fig.16

EP 1 151 962 A1

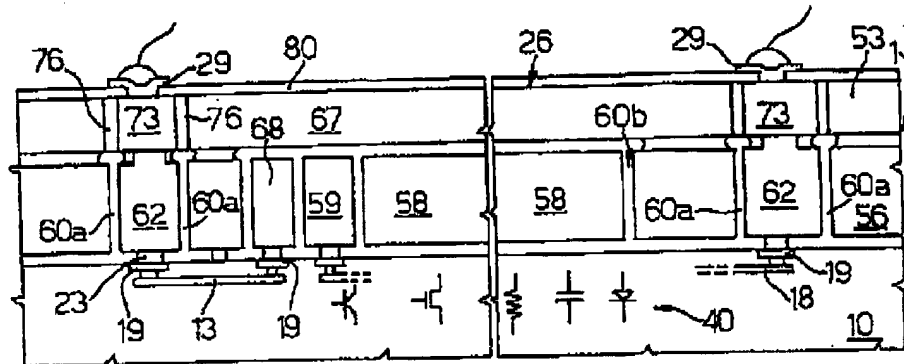


Fig.17

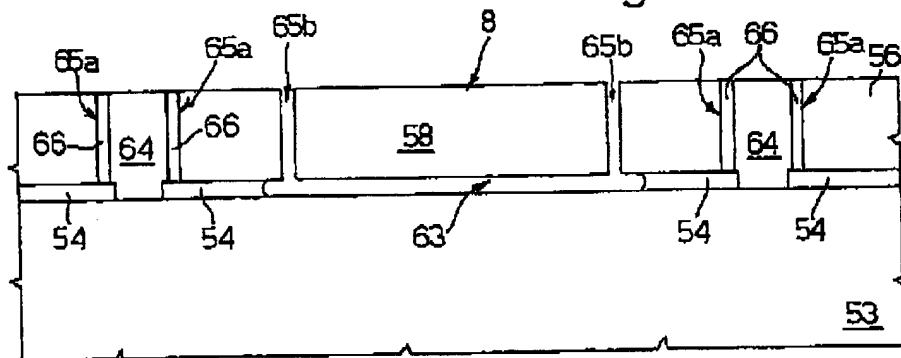


Fig.18

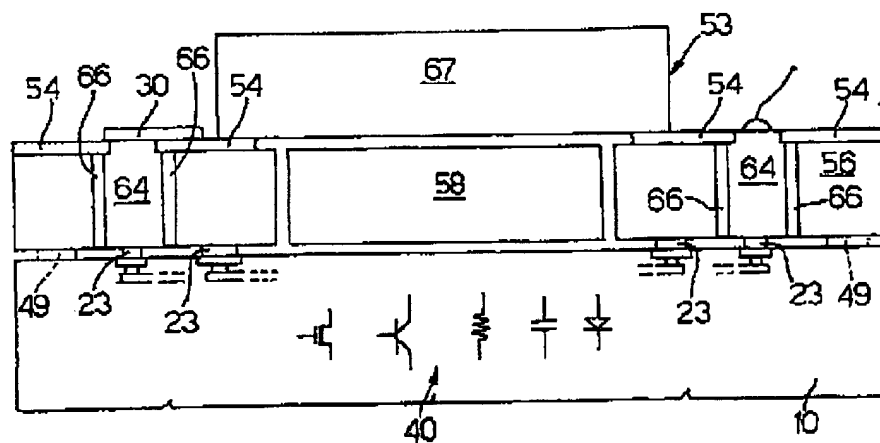


Fig.19

EP 1 151 962 A1

European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number

EP 00 83 0314

## DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Art. 57)
Y	US 4 939 568 A (TABUCHI MASAO ET AL) 3 July 1990 (1990-07-03)  * the whole document *	1-4, 6, 9, 10, 12, 18, 22-24, 29	B81C3/00 H01L25/065 H01L23/48 G11B19/20
Y	EP 0 317 084 A (GRUMMAN AEROSPACE CORP) 24 May 1989 (1989-05-24)  * the whole document *	1-4, 6, 9, 10, 12, 18, 22-24, 29	
A	US 4 660 066 A (REID LEE R) 21 April 1987 (1987-04-21) * the whole document *	1-29	
A	US 5 756 395 A (KAPoor ASHOK K ET AL) 26 May 1998 (1998-05-26) * figures *	1-29	
A	US 4 239 312 A (GRINBERG JAN ET AL) 16 December 1980 (1980-12-16)		TECHNICAL FIELDS SEARCHED (Art. 57)  B81C H01L G11B
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		8 September 2000	Prohaska, G
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date P : document cited in the application L : document cited for other reasons B : member of the same patent family, corresponding document			

EP 1 151 962 A1

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 00 83 0314

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

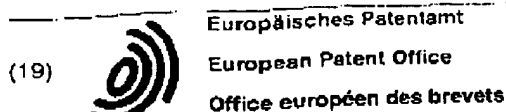
08-09-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4939568 A	03-07-1990	JP 1709516 C	11-11-1992
		JP 3074508 B	27-11-1991
		JP 62219954 A	28-09-1987
		JP 62272556 A	26-11-1987
		DE 3778944 A	17-06-1992
		EP 0238089 A	23-09-1987
		KR 9008647 B	26-11-1990
EP 0317084 A	24-05-1989	US 4784970 A	15-11-1988
		CA 1286796 A	23-07-1991
		DE 3879109 A	15-04-1993
		DE 3879109 T	17-06-1993
		JP 1168040 A	03-07-1989
		JP 2660299 B	08-10-1997
US 4660066 A	21-04-1987	NONE	
US 5756396 A	26-05-1998	US 5640049 A	17-06-1997
US 4239312 A	16-12-1980	NONE	

EPO Patent Rules

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82





(11) **EP 1 151 962 A1**

# **EUROPEAN PATENT APPLICATION**

(12)

(43) Date of publication:  
**07.11.2001 Bulletin 2001/45**

(51) Int Cl.<sup>7</sup>: **B81C 3/00, H01L 25/065,  
H01L 23/48, G11B 19/20**

(21) Application number: **00830314.1**

(22) Date of filing: **28.04.2000**

(84) Designated Contracting States:  
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU  
MC NL PT SE**  
Designated Extension States:  
**AL LT LV MK RO SI**

• Ghironi, Fabrizio  
20010 Bareggio (IT)  
• Alina, Roberto  
20010 Bareggio (IT)  
• Bombonati, Mauro  
20081 Abbiategrasso (IT)

(71) Applicant: **STMicroelectronics S.r.l.**  
**20041 Agrate Brianza (Milano) (IT)**

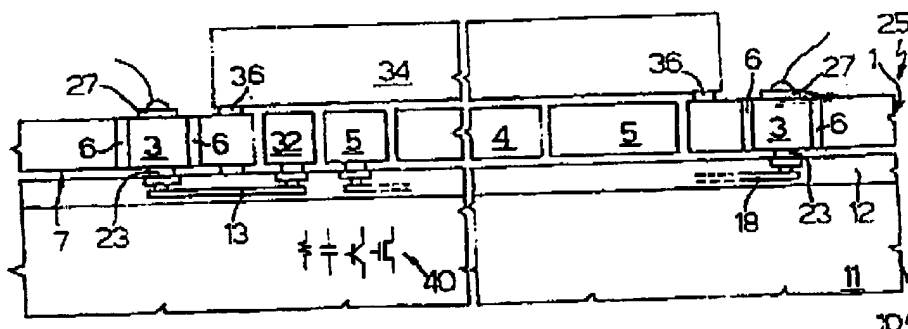
(74) Representative: **Cerbaro, Elena, Dr. et al**  
**STUDIO TORTA S.r.l.,**  
**Via Viotti, 9**  
**10121 Torino (IT)**

(72) Inventors:  
• **Mastromatteo, Ubaldo**  
**20010 Bareggio (IT)**

(54) **Structure for electrically connecting a first body of semiconductor material overlaid by a second body of semiconductor material, composite structure using the electric connection structure, and manufacturing process thereof**

(57) The electric connection structure connects a first silicon body (10) to conductive regions (29, 30) provided on the surface of a second silicon body (1) arranged on the first body (10). The electric connection structure comprises at least one plug region (3) of silicon, which extends through the second body (1); at least one insulation region (2a, 6) laterally surrounding the plug region (3); and at least one conductive electromechanical connection region (23) arranged between the first body (10) and the second body (1), and in electrical

contact with the plug region (3) and with conductive regions (15-19; 40) of the first body (10). To form the plug region (3), trenches (2a) are dug in a first wafer (1) and are filled, at least partially, with insulating material (8). Next, the plug region (3) is fixed to a metal region (23) provided on a second wafer (10), by performing a low-temperature heat treatment which causes a chemical reaction between the metal and the silicon. Subsequently, the first wafer (1) is thinned until the trenches (2a) and electrical connections (29, 30) are formed on the free face of the first wafer.



**Fig.8**

**EP 1 151 962 A1**

1

EP 1 151 962 A1

2

## Description

[0001] The present invention regards a structure for electrically connecting a first body of semiconductor material overlaid by a second body of semiconductor material, a composite structure using the electric connection structure and a manufacturing process.

[0002] In particular, the invention can be used for electrically connecting a first silicon wafer incorporating electronic components to a second silicon wafer incorporating a micromechanical structure and/or to the outside. The invention can likewise be used for electrically connecting the first wafer to a third body carried by the second wafer, as well as for connecting the first wafer to the outside when the first wafer is covered by a protection structure, and thus is not directly accessible. An example of a particular application is represented by a micro-electromechanical system including a first wafer incorporating a circuit for controlling the parameters defining the state of a micro-electromechanical structure (for example, the position of a microactuator); a second wafer incorporating the micro-electromechanical structure; and a third wafer forming a cap for protecting the micro-electromechanical structure.

[0003] Various techniques are known for mechanically connecting two semiconductor material bodies (see, for example, Martin A. Schmidt, "Wafer-to-Wafer Bonding for Microstructure Formation", Proceedings of the IEEE, Vol. 86, No. 8, August 1998). However, such techniques do not enable two or three wafers to be electrically connected, in addition to be mechanically connected, or covered components of one of the wafers to be electrically accessed.

[0004] The aim of the present invention is to provide a connection structure that enables semiconductor material bodies made on different substrates to be overlaid and to be connected mechanically and electrically together and to the outside.

[0005] According to the present invention an electric connection structure, a composite structure, and a process for manufacturing a composite structure are provided, as defined in Claims 1, 12, and 22, respectively.

[0006] For a better understanding of the present invention, preferred embodiments thereof are now described, merely to provide non-limiting examples, with reference to the attached drawings, wherein:

- Figures 1 and 2 are cross-sections through a semiconductor material wafer, in two successive manufacture steps, according to a first embodiment of the invention;
- Figure 3 shows a cross-section through the wafer of Figure 2, after bonding to a second semiconductor material wafer;
- Figure 4-6 show a cross-section of the multiwafer structure of Figure 3, in successive manufacture steps;
- Figure 7 is a perspective view of the left-hand half

of the multiwafer structure of Figure 6;

- Figure 8 shows a cross-section of the multiwafer structure of Figure 6, in a final manufacture step
- Figures 9-11 show a cross-section of a micro-electromechanical system according to a second embodiment of the invention;
- Figure 12 shows a cross-section of a composite structure formed starting from three semiconductor material substrates, according to a third embodiment of the invention;
- Figures 13 and 14 show cross-sections of a semiconductor material wafer, in two successive manufacture steps according to a fourth embodiment of the invention;
- Figure 15 shows a cross-section of the wafer of Figure 14 after bonding to a second semiconductor material wafer;
- Figure 16 shows a cross-section of a composite structure obtained from the double wafer of Figure 15, in a subsequent manufacture step;
- Figure 17 shows a cross-section of a composite wafer, according to a fifth embodiment of the invention; and
- Figures 18 and 19 show cross-sections of a composite wafer, according to a sixth embodiment of the invention, in two successive manufacture steps.

[0007] Figures 1-8 show a first embodiment of a process for manufacturing a micro-electromechanical system including a control and sensing circuitry and a micro-electromechanical sensor, for example an accelerometric sensor.

[0008] Initially, Figure 1, a first wafer 1 of semiconductor material, typically P++ or N++ doped monocrystalline silicon, sectioned along two parallel half-planes, so as to show different areas in the left-hand half and in the right-hand half, is masked and etched to form first deep trenches 2a. For example, the first wafer 1 may have a conductivity of between 5 and 15 mΩ/cm, preferably 10 mΩ/cm. As shown in Figure 2, the first trenches 2a have a closed shape and enclose monocrystalline silicon plug regions 3 intended to form through connections, as explained more clearly hereinafter.

[0009] Subsequently, the first trenches 2a are filled, either completely or partially, with insulating material 6, for example silicon dioxide. To this end, a silicon dioxide layer is deposited or grown, and is subsequently removed from a first surface 7 of the first wafer 1, to obtain the structure shown in Figure 2.

[0010] Next, Figure 3, the first wafer 1 is bonded to a second wafer 10 comprising a monocrystalline silicon substrate 11 and an insulation and/or passivation layer 12. In particular, the substrate 11 houses conductive and/or insulating regions forming electronic components for biasing the accelerometric sensor 8 and for detecting and processing electrical signals generated by the accelerometric sensor 8. As an example, Figure 3 shows conductive regions 15-16 of the N/P-type be-

3

EP 1 151 962 A1

4

longing to an electronic circuit 40, which is shown only schematically. In addition, the insulation and/or passivation layer 12 houses metal regions 13, 18, which terminate at one or both of their ends, with pad regions 19 facing the surface 22 of the second wafer 10.

[0011] Connection regions 23 are provided on the surface 22 of the second wafer 10, on top of the pad regions 19, and are of a metal that is able to react at a low temperature with the silicon of the first wafer 1 to form a gold/silicon eutectic or a metallic silicide. Typically, the connection regions 23 are made of gold, in the case where the aim is to obtain a eutectic, or of a metal chosen from among the group comprising palladium, titanium, and nickel. In the case where the aim is to obtain a silicide. Bonding regions 24 are also provided on the surface 22 and are preferably formed at the same time as the connection regions 23.

[0012] For bonding the first wafer 1 to the second wafer 10, the first wafer 1 is turned upside down so that the first surface 7 of the first wafer 1 faces the second wafer 10. The plug regions 3 of the first wafer 1 are brought into contact with the connection regions 23 of the second wafer 10, and subsequently a heat treatment at low temperature, for example 350-450°C, is carried out for a period of 30-45 min., so that the metal of the connection regions 23 of the second wafer 10 react with the silicon of the plug regions 3 and form a metallic silicide which bonds the first and the second wafers 1, 10. Thereby, a double wafer 25 is obtained, as shown in Figure 3.

[0013] Subsequently, Figure 4, the first wafer 1 is thinned from the back mechanically, for example by grinding, preferably so as to obtain a thickness of 30-40 µm. The first wafer 1 then has a second surface 26 opposite to the first surface.

[0014] Next, Figure 5, a metal layer (for example, an aluminum layer) is deposited and defined, so as to form metal regions 27 extending above the plug regions 3 and in direct electrical contact with the latter.

[0015] Subsequently, the first wafer 1 is masked and etched so as to form second trenches 2b defining an accelerometric sensor 8. In particular, as may be seen in Figures 6 and 7, the second trenches 2b separate a mobile region (forming a rotor 4) and a fixed region (forming a stator 5) from the rest of the wafer 1 and from one another. The rotor 4 is connected, through elastic connection regions (also referred to as springs 31) to fixed biasing regions 32, which are set in areas corresponding to respective connection regions 23, connected, through the metallic regions 13, to the plug regions 3.

[0016] Next, Figure 8, a cap element 34 is fixed to the wafer 1 through adhesive regions 36, in a per se known manner, and then the double wafer 25 is cut into individual dice. Finally, the metal region 27 is contacted applying the usual wire-bonding technique.

[0017] Thereby, the connection regions 23 ensures mechanical connection between the monocrystalline silicon wafers 1 and 10 and electrical connection between

the surface 22 of the second wafer 10 and the plug regions 3. In turn, the plug regions 3 allow the second wafer 10 to be contacted from above. In particular, some plug regions 3 enable the second wafer 10, not directly accessible from the front, to be connected to the outside, without requiring costly processes to be carried out from the back. In addition, as is shown in the left-hand half of Figure 8, this solution also enables connection of regions formed in the first wafer 1 to the outside. Here the rotor 4 is connected to the outside through a first connection region 23 (beneath the biasing region 32), a metal region 13, a second connection region 23 (beneath the plug region 3), and the plug region 3. The plug regions 3 are insulated by insulation regions formed by the insulating material 6 and possibly by the air present in the first deep trenches 2a, and are thus electrically insulated from the rest of the first wafer 1, except, obviously, for the regions connected to them via electric connection lines 30.

[0018] With the solution of Figures 1-8 a pressure sensor, instead of an accelerometric sensor, may be formed.

[0019] Figures 9-11 show a second embodiment of the invention regarding a unit for micrometric regulation of the read/write head of a hard-disk driver. In detail, initially the same steps are carried out as described previously with reference to Figures 1-4. After thinning the first wafer 1, an oxide layer 35 is deposited and removed selectively at the plug regions 3 to form openings 28. The second trenches 2b are then formed through the oxide layer 35 and through the wafer 1.

[0020] Subsequently, an insulating layer 38 is deposited, for example a stick foil which does not enter the second trenches 2b. The insulating layer is removed from above the openings 28, and metal connection regions are formed by depositing and defining a metal layer. In particular, in the illustrated example the metal layer fills the openings 28, where it forms contacts 29. In addition, an electric connection line 30 is formed and extends from the contact 29 arranged above the plug region 3 furthest to the right, up to above the rotor 4.

[0021] Subsequently, the composite wafer 25 is cut into dice, the insulating layer 38 is removed in oxygen plasma, and a ceramic body, referred to as slider 41, is bonded to the rotor 4 in a per se known manner (Figure 11). The slider 41 carries a transducer 42 for data reading/writing on a hard disk (not shown). The transducer 42 is electrically contacted through connection regions 43, one of which may be seen in Figure 11, which are formed directly on one side of the slider 41. Each connection region 43 extends from the transducer 42 as far as a pad 44 in electrical contact with an electric connection line 30.

[0022] Thereby, the plug region 3 furthest to the right enables electrical connection between the transducer 42 on the slider 41 and the electrical circuit 40, which can thus transmit to the transducer 42 the data to be written, or process the signal picked up by the transducer.

3

EP 1 151 962 A1

er 42. In addition, in a known manner, the electrical circuit 40 controls movement of the rotor 4, and consequently of the slider 41. Finally, a connection via an intermediate plug region (not shown) enables connection of the electrical circuit 40 to the outside in a way similar to that illustrated in the right-hand part of Figure 8.

[0023] Consequently, also in this case the plug regions 3 enable connection of non-accessible regions of the second wafer 10 to elements arranged above them (here, the transducer 42), as well as to the outside.

[0024] Figure 12 shows a third embodiment regarding the manufacture of circuits or structures to be kept in vacuum conditions. In the illustrated example, the wafer 1, after forming the plug regions 3 by digging the first trenches 2a and filling them with insulating material 6, has been bonded to a second wafer 10, wherein a filter 48 has been previously made, for example of the band-pass type for high frequencies. The first wafer 1 is bonded to the second wafer 10, not only through the connection regions 23, but also through a sealing region 49 which extends between the first wafer 1 and the second wafer 10, and completely surrounds the area in which the filter 48 is formed, as well as the plug regions 3. The sealing region 49 is, for example, made using a low-melting glass and has a closed shape. If bonding of the first wafer 1 and second wafer 10 is carried out in a low-pressure environment, the filter 48 remains vacuum encapsulated.

[0025] Next, the first wafer 1 is thinned as described above, and the double wafer 1, 10 is cut into dice 50. The dice 50 are then bonded to a third wafer 51 which houses a circuit 52 and which has previously been provided with connection regions 23a similar to the connection regions 23. The thinned side of the first wafer 1 faces the third wafer 51, and the plug regions 3 must be aligned to the connection regions 23a.

[0026] In this case, the first wafer 1, in addition to protecting and isolating the filter 48 from the outside environment and maintaining it in vacuum conditions, enables its electrical connection with the circuit 52 incorporated in the third wafer 51. In addition, it is possible to carry out electrical testing of the circuit 52 connected to the filter 48 at the wafer level (EWS-Electric Wafer Sort test).

[0027] Figures 13-16 show a fourth embodiment of the invention. According to Figure 13, initially the first wafer 1 comprises a substrate 53 accommodating first trenches 72a, and the first trenches 72a are filled with insulating material 76 to insulate first plug portions 73, in a way similar to that described with reference to Figure 1 for the plug regions 3. Then a sacrificial layer 54, for example of silicon dioxide, is deposited or grown, then is masked and etched so as to form openings 55 on top of the first plug portions 73 and in areas where anchorages with the structure on top are to be made, as described hereinafter.

[0028] Subsequently (Figure 14), a polycrystalline silicon seed layer is deposited on top of the sacrificial layer.

54 and in the openings 55, and then a polycrystalline silicon epitaxial layer 56 is grown. In this way, the epitaxial layer 56 is in direct contact with the substrate 53 at the openings 55. Next, inside the epitaxial layer 56 third and fourth trenches 60a, 60b are dug, which reach as far as the sacrificial layer 54.

[0029] In particular, the third trenches 60a delimit second plug portions 62 aligned vertically with the first plug portions 73 in the substrate 53, and the third trenches 60a define a desired micromechanical structure (in the example illustrated, a microactuator 57 of the rotating type, comprising a rotor 58 and a stator 59, with the rotor 58 supported by springs, which are not illustrated).

[0030] Subsequently, in a known way, a part of the sacrificial layer 54 is removed through the fourth trenches 60b. In particular, the sacrificial layer 54 is removed beneath the rotor 58 to form an air gap 63, and it substantially remains underneath the stator 59. The sacrificial layer 54 is removed only to a very small extent through the third trenches 60a, given the different geometry (the micromechanical structure is formed by thin regions and/or perforated regions, allowing the sacrificial layer 54 to be substantially removed; this, instead, is not done through the third trenches 60a).

[0031] In a way not shown, it is then possible to fill the third trenches, at least partially, with insulating material, in a way similar to that described for the first trenches 2a of Figure 1.

[0032] Subsequently (Figure 15), the first wafer 1 is turned upside down and bonded to the second wafer 10, inside which components of the circuit 40 have already been formed, and on top of which the connection regions 23 have already been made. Also in this case, a low-temperature heat treatment is carried out to enable a chemical reaction between the silicon of the epitaxial layer 56, at the second plug portions 62, and the metal of the connection regions 23. Next, the substrate 53 of the first wafer 1 is thinned until the insulating material 76 (or at least the bottom of the first trenches 72a) is reached, an oxide layer 35 is deposited, the openings 28 are formed in the oxide layer 35, and then second trenches 72b are made which separate fixed parts from mobile parts in the substrate 53.

[0033] Next, as has been described with reference to Figure 10, an insulating layer (stick foil) is deposited and selectively removed, and the electrical contacts 28 and electric connection lines 30 are formed. In Figure 16, an electric connection line 30 connects the portion of the substrate 53 to which the rotor 58 is anchored (cap region 67) to the first plug region 73 that is furthest to the left, thus enabling electrical connection of the rotor 58 to the circuit 40 through the cap region 67, the first plug portion 73 on the left, and the second plug portion 62 on the left. Shown in the right-hand half of Figure 16 is instead the electrical connection between the circuit 40 and the outside, through the second plug portion 62, the first plug region 73, and the connection region 23 on the right.

[0034] Subsequently, the insulating layer is removed, and a body to be moved, for example a slider similar to the slider 41 of Figure 11, can be fixed to the cap region 67.

[0035] The solution shown in Figures 13-16 thus provides a micromechanical structure 57 protected by a cap (cap region 67) and easily connects the circuit 40 both to the micromechanical structure 57 and to the outside.

[0036] Figure 17 shows a variation of the structure of Figure 16, in which the rotor 58 is not anchored to the substrate 53, but is supported by springs (not shown) and biasing regions 60, similar to the biasing regions 31, 32 of Figure 7. In addition, the cap region 67 is fixed and does not have the second trenches 72b. The rotor 58 and stator 59 are connected via connection regions 23 and pad regions 19 to metallic regions 13, 18 formed in the second wafer 10. The metallic regions 13 are connected to the outside (as shown in the left-hand half of Figure 17) via further connection regions 23 aligned with plug regions 62, 73 formed in the first wafer 1, in a way similar to that described with reference to Figures 13-16, and via contacts 29. In addition, the metallic regions 18 enable connection of the circuit 40 to the stator 59 and, via plug regions 62, 73 and contacts 29, to the outside, as shown in the right-hand half of Figure 17. An insulating layer 80 covers the surface 26 of the first wafer 1.

[0037] Figures 18 and 19 show a sixth embodiment, in which a micromechanical structure, for example an accelerometric sensor 8, is protected by a cap and electrically connected to the biasing and sensing circuit via plug regions.

[0038] Initially (Figure 18), the first wafer comprises a substrate 53, which, in contrast to the previous embodiments, is not etched to form trenches. On the substrate 53, a sacrificial layer 54 is deposited and defined, and is removed only at openings 55. Next, a polycrystalline silicon seed layer is deposited, and the epitaxial layer 56 is grown, as described with reference to Figure 14.

[0039] The epitaxial layer 56 is etched to form fifth trenches 65a for delimiting second plug portions 64. Here, the fifth trenches 65a are filled, either partially or completely, with insulating material 66, sixth trenches 65b are formed for defining the accelerometric sensor 8, and the sacrificial layer 54 is partially removed through the sixth trenches 65b, so as to free the rotor 58 of the accelerometric sensor 8. As for the embodiment shown in Figures 1-8, the rotor 58 is carried by the fixed part via springs (not illustrated).

[0040] Subsequently, the first wafer 1 is bonded to the second wafer 10 using the connection regions 23 already formed on the surface 22 of the second wafer 10. Then the first wafer 1 is thinned by grinding until the desired thickness for the substrate 53. Next, the substrate 53 is selectively removed so as to form a cap region 67 of larger dimensions than the rotor 58, but of smaller dimensions than the chip housing the circuit 40, obtained after cutting the wafers 1, 10. In this way, the cap region 67 covers the rotor 58 from the back (protecting

it mechanically), but leaves the plug regions 64 free.

[0041] Finally, the contacts 29 and the electric connection lines 30 are formed, which, in this embodiment, contact directly the silicon of the epitaxial layer 54. In particular, in the example illustrated in Figure 19, an electric connection line 30 connects a region (not shown), arranged inside the fixed part and is electrically connected to the rotor 58, to the plug region 64 on the left, and thus to the circuit 40. A ball-and-wire connection on the right instead enables connection of the circuit 40 to the outside.

[0042] When the accelerometric sensor 8 is to be kept at low pressure, for example to reduce friction with air during movement, a sealing region 49 may be provided which surrounds the area of the accelerometric sensor 8, then the first wafer 1 may be bonded to the second wafer 10 in vacuum conditions, as already described with reference to Figure 12.

[0043] The advantages of the process and structures described are evident from the above. In particular, it is emphasized that they enable mechanical connection of two bodies of semiconductor material, in particular of monocrystalline silicon, arranged on one another, and at the same time the electrical connection of a structure or circuit formed in the underlying body (covered by the overlying body) to the outside or to a structure made in the overlying body; or else, they enable electrical connection of the underlying body to regions arranged above the overlying body, without requiring complicated and costly processes to be carried out from the back, without damaging the structures and circuits already made, and applying single manufacture steps that are commonly used in the manufacture of wafers of semiconductor material for forming micro-electromechanical structures.

[0044] The described solutions moreover make it possible, when necessary, to isolate preset areas of the underlying body and/or of the overlying body from the outside environment, for example to enclose delicate elements in a low-pressure environment, and/or to isolate and prevent contamination of these elements during manufacture (for example, cutting semiconductor material wafers), during subsequent manipulation steps, and during use.

[0045] Finally, it is clear that numerous modifications and variations may be made to the connection structure, the composite structure, and to the manufacture process described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. In particular, it is emphasized that the present connection structure may be used for a wide range of applications, both for the connection of electronic circuits integrated in two or more different substrates, and for the connection of micro-electromechanical structures of various kinds to biasing/control/sensing circuits associated to the micro-electromechanical structures. The present connection structure may be used for connecting a high number of substrates, according to the re-

EP 1 151 962 A1

10

quirements and to general considerations of a mechanical/electrical nature.

#### Claims

1. An electric connecting structure for connecting a first body (10) of semiconductor material overlaid by second body (1) of semiconductor material, characterized by:

at least one plug region (3; 73, 62; 64) extending through a portion of said second body (1) and made of semiconductor material;  
at least one insulation region (2a, 6; 60a, 72a, 76; 65a, 66) surrounding laterally said plug region (3; 73, 62; 64); and  
at least one first electromechanical connection region (23) of electrically conductive material arranged between said first body (10) and said second body (1) and in electrical contact with said plug region (3; 73, 62; 64) and with conductive regions (15-19; 40) of said first body (10).

2. The electric connection structure of Claim 1, characterized in that said plug region (3; 62, 73) extends throughout the thickness of said second body (1) and has a first face and a second face, said first face being in contact with said first electromechanical connection region (23);  
and comprising at least one contact region (27; 29; 23a) of electrically conducting material, in contact with said second face of said plug region.

3. The electric connection structure of Claim 2, characterized by an electric connection line (30) extending above said second body (1) and having a first end forming said contact region (29).

4. The electric connection structure of Claim 3, characterized in that said electric connection line (30) has a second end in electrical contact with a conductive region of said second body (1).

5. The electric connection structure of Claim 3, characterized in that said electric connection line (30) has a second end in electrical contact with a contact region (44) formed on a third body (41) fixed to said second body (1).

6. The electric connection structure of Claim 2, for electrically connecting said second body (1) to a third body (51) of semiconductor material arranged on said second body (1), characterized in that said contact region comprises at least one second electromechanical connection region (23a) made of a material resulting from the chemical reaction of said

semiconductor material with a metal, said second electromechanical connection regions (23a) being arranged between said second body (1) and said third body (51)

7. The electric connection structure of Claim 1, for a second body (1) comprising a substrate region (53) and an epitaxial region (56) arranged on each other and partially insulated from one another by insulating regions (54, 63),  
characterized in that said plug region (62, 73) comprises a first plug portion (73) extending throughout the thickness of said substrate region (53), and at least one second plug portion (62) formed inside said epitaxial region (56), said second plug portion (62) being aligned and in direct electrical contact with said first plug portion (73);

said insulation region (60a, 72a, 76) comprises a first insulation portion (72a, 76) laterally surrounding said first plug portion (73), and a second insulation portion (60a) laterally surrounding said second plug portion (62);  
at least one contact region (29) of electrically conducting material extends on a free face (26) of said substrate region (53) in electrical contact with said first plug portion (73);  
and said second plug portion (62) faces and is in direct electrical contact with said first electromechanical connection region (23).

8. The electric connection structure of Claim 1, for a second body (1) comprising a substrate region (67) and an epitaxial region (56) arranged on one another and reciprocally insulated by insulating regions (54, 63),  
characterized in that said substrate region (67) has a smaller area than said epitaxial region (56), said plug region (64) extends throughout the thickness of said epitaxial region (56), is not aligned with respect to said substrate region (67), and has a first face and a second face, said first face being in contact with said first electromechanical connection region (23), and said second face being in direct contact with at least one electric connection region (30) of electrically conducting material.

9. The electric connection structure according to any of the foregoing claims, characterized in that said insulation region (2a, 6; 60a, 72a, 76; 65a, 66) comprises a trench having a closed shape filled at least partially with insulating material (6; 66; 76).

10. The electric connection structure according to any of the foregoing claims, characterized in that said first electromechanical connection region (23) is made of a material resulting from the chemical reaction of said semiconductor material with a metal.

11

EP 1 151 962 A1

12

11. The electric connection structure according to any of the foregoing claims, characterized in that said first electromechanical connection region (23) is made of a metal resulting from the chemical reaction of silicon with a metal chosen from among a group comprising gold, palladium, titanium, and nickel.
12. A composite structure comprising a first body (1) of semiconductor material, a second body (10) of semiconductor material arranged on said first body (1), and an electric connection structure, characterized in that said electric connection structure is formed according to any of Claims 1-11.
13. A composite structure comprising a first body (10) of semiconductor material, a second body (1) of semiconductor material arranged on said first body (10), and an electric connection structure according to Claim 2, characterized in that said first body (10) houses an electronic circuit (15-19; 40), and said second body (1) houses a micro-electromechanical device (8; 57) comprising a fixed part (1, 5, 32; 56, 59, 68) and a mobile part (4; 58) separated from each other by at least one delimitation trench (2b) extending through said second body (1).
14. The composite structure of Claim 13, characterized in that an external electric connection wire is bonded to said contact region (29).
15. The composite structure of Claim 13, characterized in that said electric connection structure comprises an electric connection line (30) extending above said second body (1) and having a first end forming said contact region (29), and a second end in electrical contact with said micro-electromechanical device (8; 57).
16. The composite structure of Claim 13, characterized by a third body (41) fixed to said second body (1), said electric connection structure comprising an electric connection line (30) having a first end forming said contact region (29) and a second end in electrical contact with a contact region (44) formed on said third body (41).
17. The composite structure of Claim 16, characterized in that said third body (41) is a slider, and in that said composite structure forms an actuator unit for micrometric position regulation of a hard-disk driver.
18. A composite structure comprising a first body (10) of semiconductor material, a second body (1) of semiconductor material arranged on said first body, a third body (51) of semiconductor material fixed to said second body, and an electric connection structure according to Claim 6 characterized in that said first body (10) and said third body (51) house a respective electronic circuit (48, 52), said electronic circuits being connected together through said plug region (3).
19. The composite structure of Claim 18, characterized by a sealing region (49) having a closed shape and arranged between said first and said second bodies (10, 1), outside said electronic circuit (48).
20. A composite structure comprising:  
a first body (10) of semiconductor material;  
a second body (1) of semiconductor material arranged on said first body and comprising a substrate region (53) and an epitaxial region (56), overlaid to each other and partially insulated from one another by insulating regions (54, 63); and  
an electric connection structure according to Claim 7,  
characterized in that said epitaxial region (56) houses a micro-electromechanical device (57) comprising a fixed part (59, 68) and a mobile part (58) separated from one another by at least one delimitation trench (60b) extending through said epitaxial region (56), and in that said substrate region (53) forms a cap region (67).
21. A composite structure comprising:  
a first body (10) of semiconductor material;  
a second body (1) of semiconductor material arranged on said first body and comprising a substrate region (67) and an epitaxial region (56), overlaid to each other and insulated from one another by insulating regions (54, 63), said substrate region (67) having a smaller area than said epitaxial region (56); and  
an electric connection structure according to Claim 8,  
characterized in that said epitaxial region (56) houses a micro-electromechanical device (8) comprising a fixed part (59) and a mobile part (58) separated from one another by at least one delimitation trench (65b) extending through said epitaxial region (56), and in that said substrate region forms a cap region (67) which has larger dimensions than said mobile part (58) and is fixed to said fixed part (59).
22. A process for manufacturing a composite structure, characterized by the steps of:  
forming at least one plug region (3; 73, 62; 64)

13

EP 1 151 962 A1

14

surrounded by an insulation region (2a, 6; 60a, 72a, 76; 65a, 66) extending through a first wafer (1) of semiconductor material;

forming at least one electromechanical-connection region (23) of conductive material on a second wafer (10) of semiconductor material, and aligned with said plug region;

bringing said first wafer (1) and said second wafer (10) close together, bringing said plug region (3; 73, 62; 64) into contact with said electromechanical-connection (23); and  
fixing said first wafer and said second wafer through said electromechanical connection region.

23. The process of Claim 22, characterized by the steps of:

Initially forming said insulation region (2a, 6) in said first wafer (1), said insulation region partially extending inside said first wafer from a surface (7) of said first wafer and laterally delimiting said one plug region (3);  
turning said first wafer (1) upside down to bring said surface (7) of said first wafer in a facing position with said second wafer (10); and  
thinning said first wafer (1) until said insulation region (2a, 6).

24. The process of Claim 23, characterized in that said step of forming said insulation region (2a, 6) comprises the steps of:

forming isolation trenches (2a) in said first wafer (1); and  
at least partially filling said isolation trenches with insulating material (6).

25. The process of Claim 24, characterized by the step of forming trenches (2b) delimiting a micro-electromechanical structure (8) in said first wafer (1), and forming an electronic circuit (13-19) in said second wafer (10) before forming said electromechanical-connection region.

26. The process of Claim 22, characterized by the steps of:

forming a first insulation portion (72a, 76) of said insulation region in a substrate (53) of semiconductor material, said first insulation portion (72a, 76) partially extending inside said substrate from a surface of said substrate, and laterally delimiting a first plug portion (73) of said plug region;  
growing an epitaxial layer (56) from said surface of said substrate (53);  
forming at least one second insulation portion

(60b) of said insulation region in said epitaxial layer (56), said second insulation portion (60b) extending throughout the thickness of said epitaxial layer and

delimiting a second plug portion (62) of said plug region which is substantially aligned and in electrical contact with said first plug portion (73);

fixing said second plug portion (62) to said second wafer (10);

thinning said substrate (53) until said first insulation portion (72a, 76); and

forming contact regions (29, 30) on a free face of said substrate (53).

27. The process of Claim 22, characterized by the steps of:

on a substrate (53), growing an epitaxial layer (56);

forming said insulation region (65a, 66) in said epitaxial layer (56), said insulation region (65a, 66) extending throughout the thickness of said epitaxial layer and delimiting said plug region (64);

forming a device (57) to be protected in said epitaxial layer (56);

fixing said epitaxial layer (56) of said first wafer (1) to said second wafer (10) through said plug region (64); selectively removing said substrate (53) to form a cap region (67) covering said device (57) to be protected, and freeing said plug region (64); and

forming contact regions (29, 30) above said plug region (64).

28. The process according to any of Claims 22-27, characterized in that said step of fixing said first wafer (1) to said second wafer (10) is carried out in vacuum conditions and further comprises the step of forming a sealing region (49) between said first wafer (1) and said second wafer (10).

29. The process according to any of Claims 22-28, characterized in that said conductive material of said electromechanical connection region (23) is a metal, and in that said fixing step comprises the step of causing said metal of said electromechanical-connection structure (23) to react with said semiconductor material of said plug region (3; 62; 64).



EP 1 151 962 A1

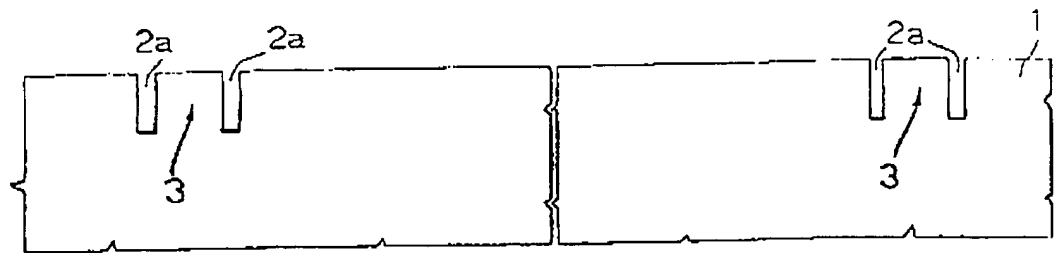


Fig. 1

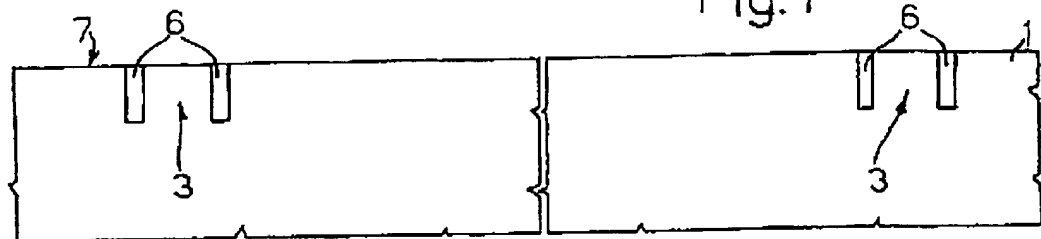


Fig. 2

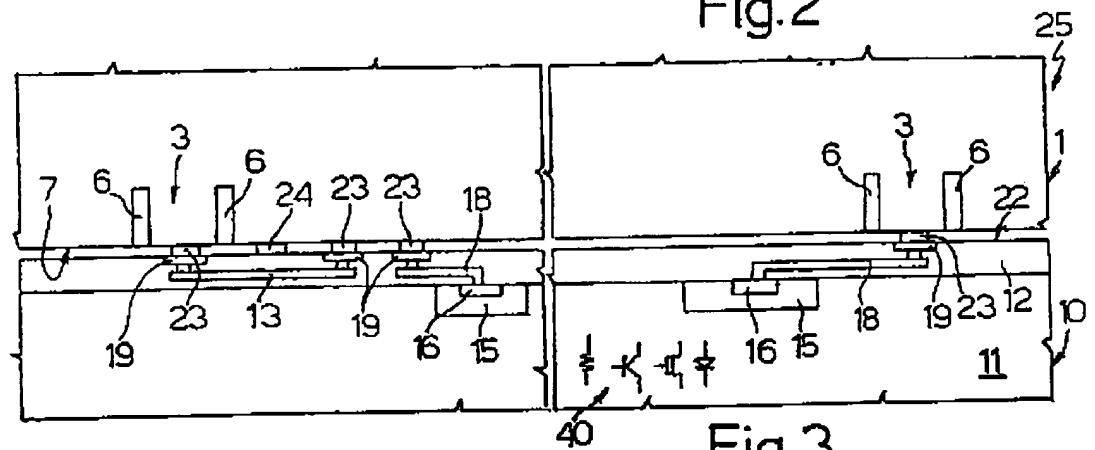


Fig. 3

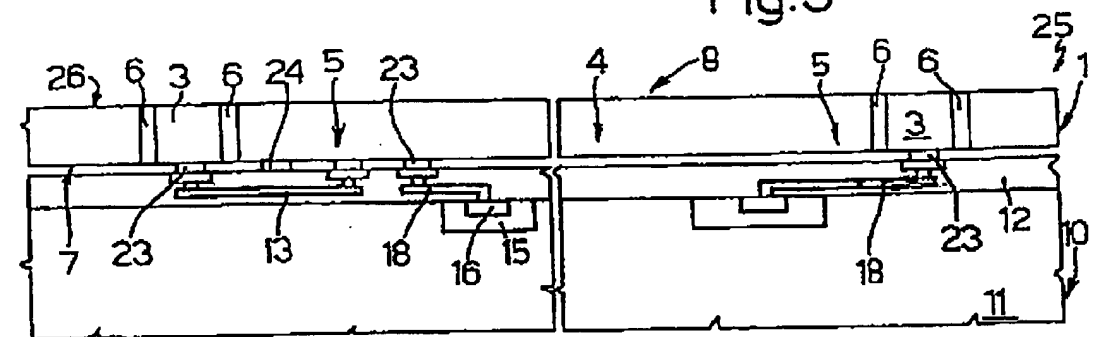


Fig. 4

EP 1 151 962 A1

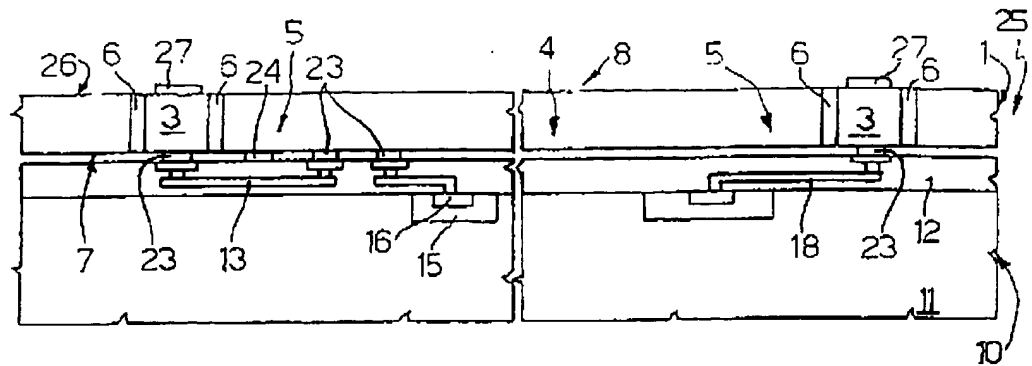


Fig. 5

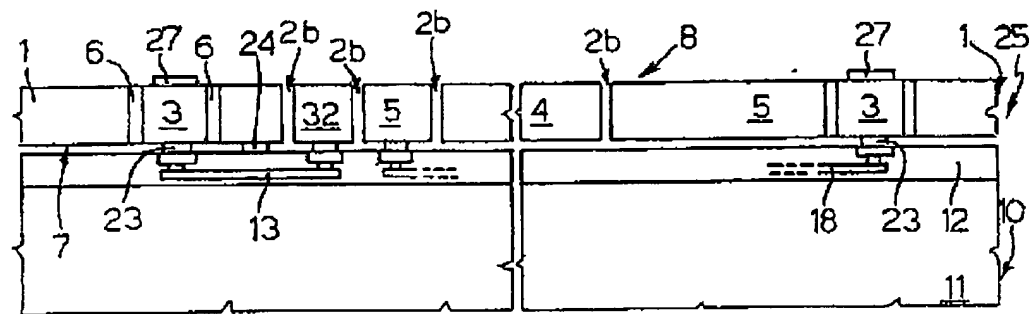


Fig. 6

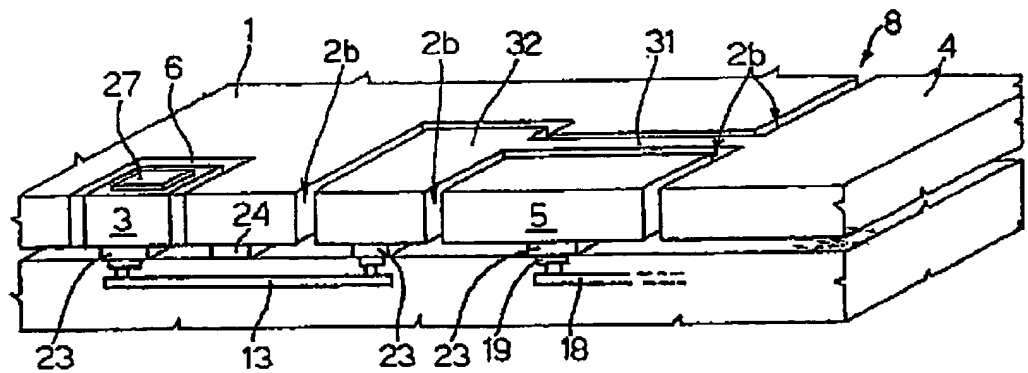


Fig. 7

EP 1 151 962 A1

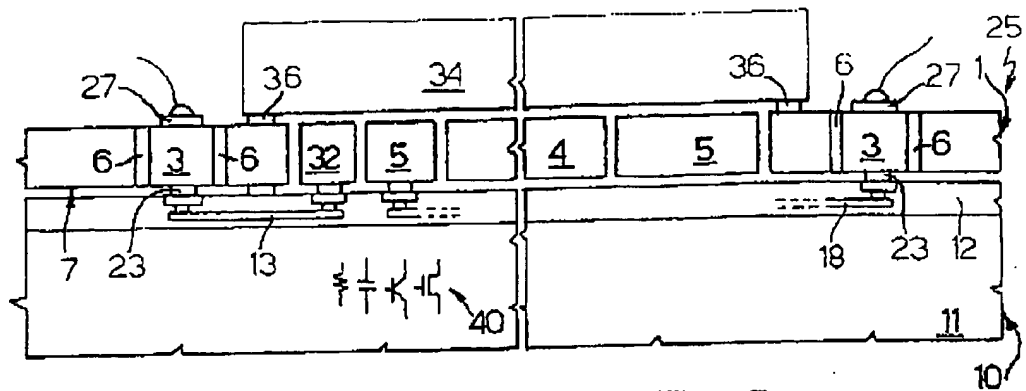


Fig.8

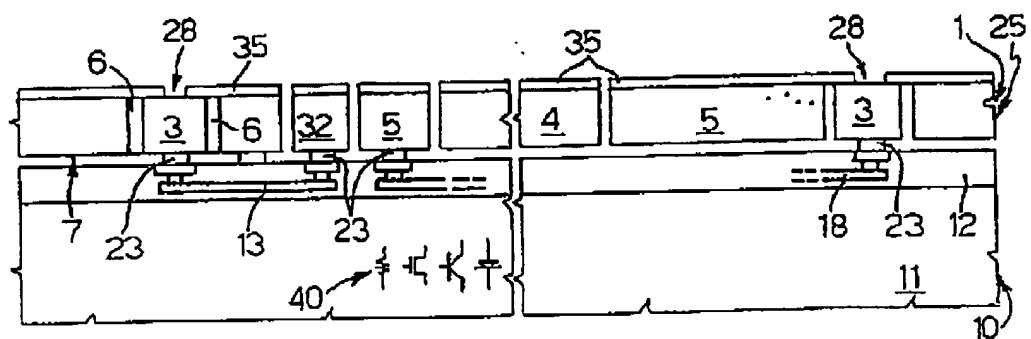


Fig.9

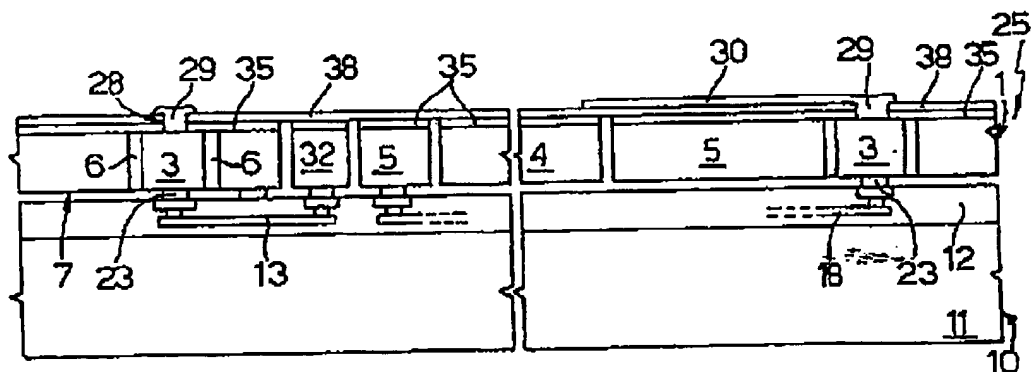


Fig.10

EP 1 151 962 A1

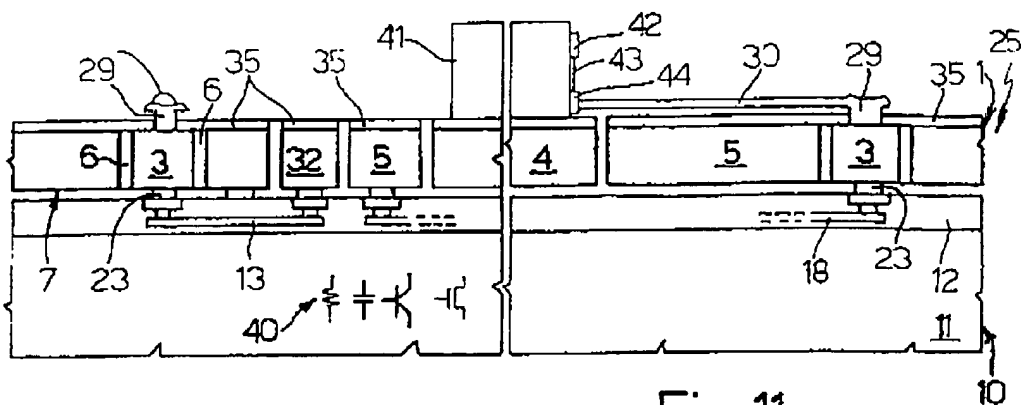


Fig. 11

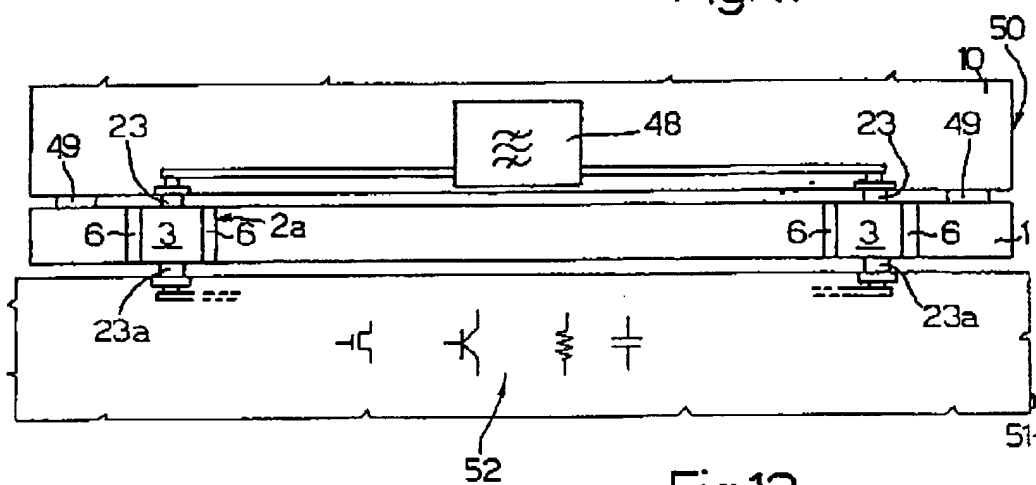


Fig. 12

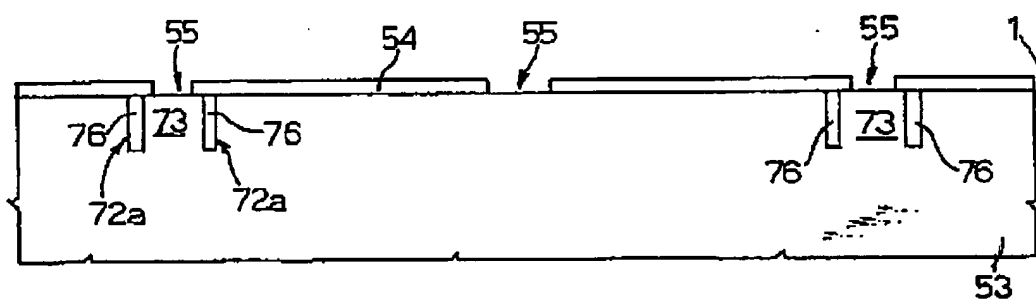


Fig. 13

EP 1 151 962 A1

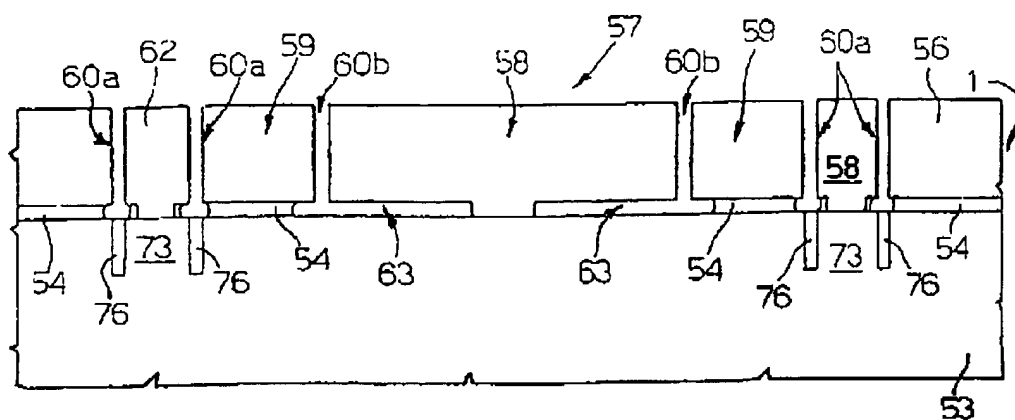


Fig. 14

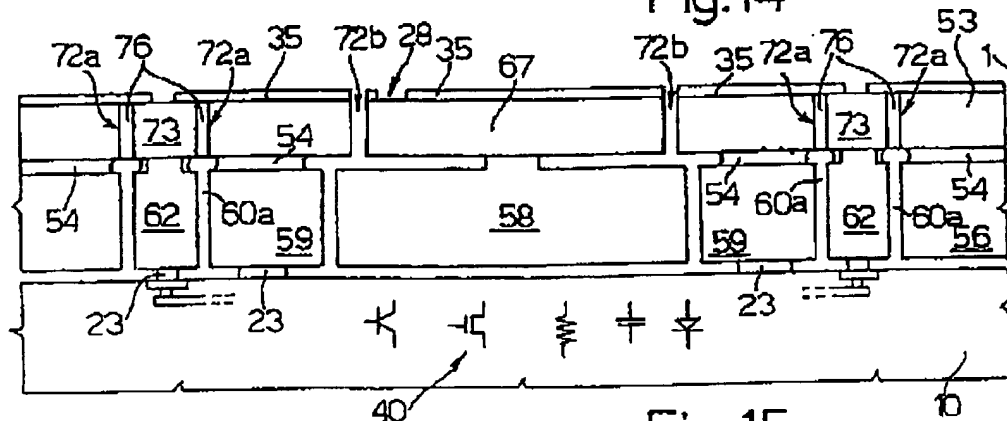


Fig. 15

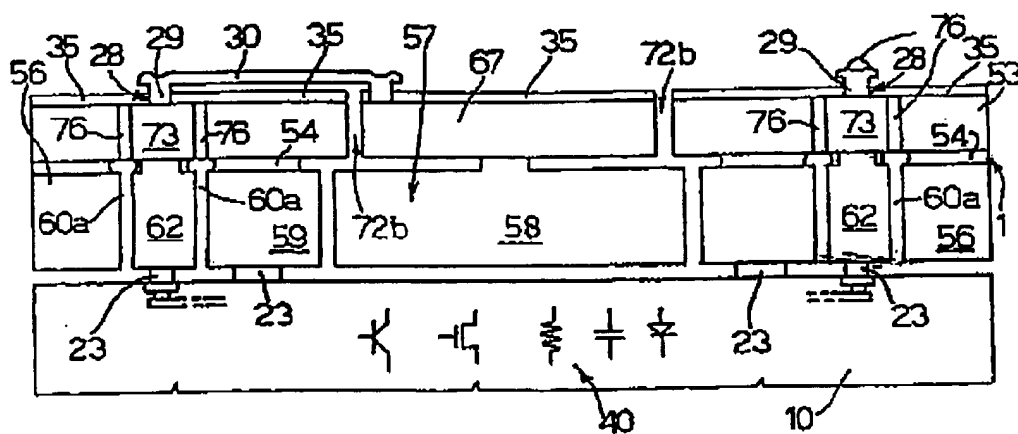


Fig. 16

EP 1 151 962 A1

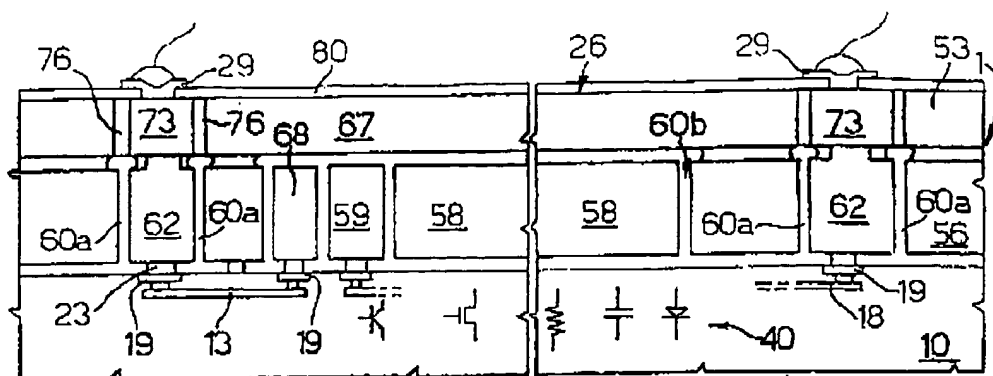


Fig. 17

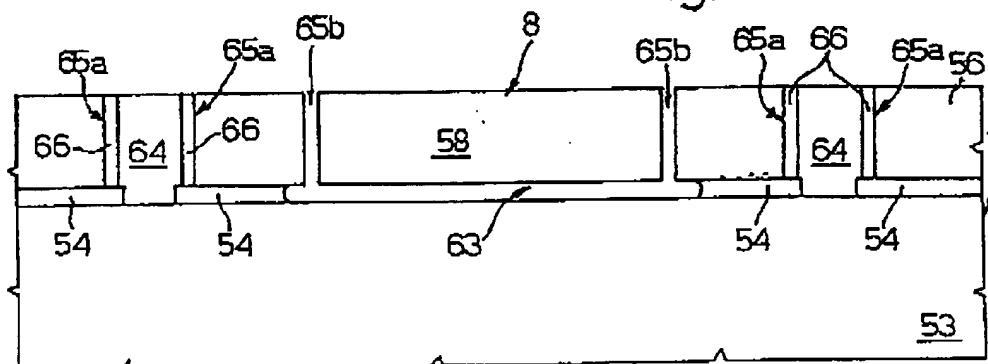


Fig. 18

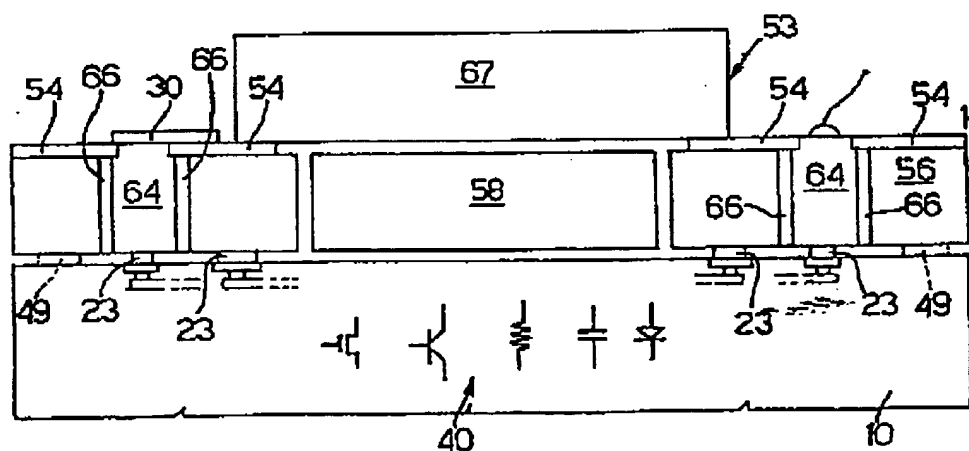


Fig. 19

EP 1 151 962 A1

European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 00 83 0314

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (art.61)
Y	US 4 939 568 A (TAGUCHI MASAO ET AL) 3 July 1990 (1990-07-03)  * the whole document *	1-4, 6, 9, 10, 12, 18, 22-24, 29	B81C3/00 H01L25/065 H01L23/48 G11B19/20
Y	EP 0 317 084 A (GRUMMAN AEROSPACE CORP) 24 May 1989 (1989-05-24)  * the whole document *	1-4, 6, 9, 10, 12, 18, 22-24, 29	
A	US 4 660 066 A (REID LEE R) 21 April 1987 (1987-04-21) * the whole document *	1-29	
A	US 5 756 395 A (KAPOOR ASHOK K ET AL) 26 May 1998 (1998-05-26) * figures *	1-29	
A	US 4 239 312 A (GRINBERG JAN ET AL) 16 December 1980 (1980-12-16)		TECHNICAL FIELDS SEARCHED (art.61)  B81C H01L G11B
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>8 September 2000</b>	Examiner <b>Prohaska, G</b>
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date I : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EP 1 151 962 A1

# ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 00 83 0314

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

08-09-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4939568 A	03-07-1990	JP 1709516 C	11-11-1992
		JP 3074508 B	27-11-1991
		JP 62219954 A	28-09-1987
		JP 62272556 A	26-11-1987
		DE 3778944 A	17-06-1992
		EP 0238089 A	23-08-1987
		KR 9008647 B	26-11-1990
EP 0317084 A	24-05-1989	US 4784970 A	15-11-1988
		CA 1286796 A	23-07-1991
		DE 3879109 A	15-04-1993
		DE 3879109 T	17-06-1993
		JP 1168040 A	03-07-1989
		JP 2660299 B	08-10-1997
US 4660066 A	21-04-1987	NONE	
US 5756395 A	26-05-1998	US 5640049 A	17-06-1997
US 4239312 A	16-12-1980	NONE	

EPO FORM PUST

For more details about this annex: see Official Journal of the European Patent Office, No. 12/82



**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

☐ **BLACK BORDERS**

☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**

☐ **FADED TEXT OR DRAWING**

☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**

☐ **SKEWED/SLANTED IMAGES**

☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**

☐ **GRAY SCALE DOCUMENTS**

☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**

☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**

☐ **OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**